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High power 510 GHz monolithic integrated frequency tripler for local oscillation sources in heterodyne receiver

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Abstract: A high power 490~530 GHz monolithic integrated frequency tripler is demonstrated based on Gallium Arsenide material. Based on the proposed symmetrical and balanced configuration, the tripler could not only achieve good amplitude and phase balances for efficient power synthesis, but also provide a DC bias path without any bypass capacitor to ensure efficient frequency doubling efficiency. Tolerance simulations are also carried out to analyze the effects of key electrical and structural parameters of the diode on the frequency doubling performance in order to maximize the frequency doubling performance. Finally, the developed 510 GHz triplet, driven by approximately 80-200 mW input power, has an output power of 4-16 mW in the frequency range of 490~530 GHz, where the peak frequency doubling efficiency is 11%. At the 522 GHz frequency point, the triplex produces a maximum output power of 16 mW driven by an input power of 218 mW. The triplexer will later be used as the local oscillator source of a 1 THz solid-state external super outlier mixer.

Key words: electronic technology, terahertz tripler, monolithic integrated circuit, Schottky diode, local oscillator

用于超外差接收机提供本振源的高功率510 GHz单片集成三倍频器

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摘要:本文介绍了一种基于砷化镓材料的高功率490~530 GHz单片集成三倍频器。基于提出的对称平衡结构,该三倍频器不仅可以实现良好的振幅和相位平衡,用来实现高效的功率合成,还可以在没有任何旁路电容的情况下提供直流偏置路径以保证高效倍频效率。同时,开展容差性仿真分析二极管关键电气参数与结构参数对倍频性能的影响研究,以便最大化提升倍频性能。最终,在大约80~200 mW的输入功率驱动下,研制的510 GHz三倍频,在490~530 GHz频率范围内,输出功率为4~16 mW,其中峰值倍频效率11%。在522 GHz频点处,该三倍频在218 mW的输入功率驱动下,产生16 mW的最大输出功率。该三倍频器后期将用于1 THz的固态外超外差混频器的本振源。

关 键 词:电子技术;太赫兹倍频器;单片集成电路;肖特基二极管;本振源

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Introduction

Over the past years, compact and robust local oscillators based on Schottky-based frequency multipliers for heterodyne receivers and spectrograph have provided enormous astronomy observations in the range of 0. 1-10 THz, including stellar origins and evolution as well as molecular clouds[1-5]. So far, developments of the heterodyne receiver channels at frequencies ranging from 183 GHz up to 1910 GHz certainly contribute to the extraordi-

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nary results achieved in the Heterodyne Instrument for the Far-Infrared (HIFI) on-board ESA's Herschel Space Observatory and Ice Cloud Imager (ICI) for MetOp Second Generation (MetOp-SG) satellites. Thus, the coming array applications with high resolution based on multi-pixel heterodyne receivers in terahertz range up to 1.9 THz put forward the enormous demand for high power sources provided by Schottky-based multipliers over 500 GHz.

Generally, terahertz multiplier sources are typically composed of a series of doublers and triplers to achieve the desired output frequency[6-8]. In the most commonly used balanced biased tripler circuits[8], all diodes should be in series connection with one arm connected to the ground and another to an on-chip capacitor to form a virtual loop at RF as well as DC path, as shown in Fig. 1. With the help of on-chip capacitor and perfect schottky diode, the JPL on-chip power combing circuit based on the traditional tripler topology is a typical and successful case. A series of state-of-the-art high power schottky diode based tripler are achieved, such as 35 mW 335 GHz tripler (14 peak efficiency), 30 mW 528 GHz tripler (9% peak efficiency), and 0.8 mW 1.6 THz tripler (3.5% peak efficiency). Through high thermal conductivity substrate, other 7~13 mW terahertz sources around 500 GHz are fabricated, and tested[9-10].

However, the traditional design of Schottky-diode balanced tripler has two inherent limits. On the one hand, small asymmetries are inevitable and introduced by the physical structure of series diode and cause imbalance of input and output coupling per diode, which would influence the performance of this quasi-symmetrical tripler[8],[11]. On the other hand, the doubling performance of the tripler in Fig. 1 absolutely relys on the on-chip bypass capacitor, which provides the RF grounding and DC biasing path at the same time. Thus, the non-ideality of bypass capacitor leads to the circuit asymmetry, which would introduce the unwanted imbalance effect and reduce the conversion efficiency as a result[12]. In 2003, Kamaljeet S. Saini[13] has proved the equivalent series resistances and Q factor of integrated capacitors are 3.5~20.3 Ω and 2~7.2, respectively. Thus, to fend off this issue, several un-biased schemes without bypass capacitor for balanced frequency tripler have been presented in recent years. However, these configurations always require coupled lines to guarantee the diodes in reverse polarity, which suffer limited bandwidth and conversion efficiencies[14]. Meanwhile, to further increase output power at terahertz frequency range, power-combined scheme with multiple chips is commonly adopted. However, not only the power combining topologies based traditional tripler could not throw away the inherent limits as mentioned above, but also the use of several Y-junctions increases unnecessarily the waveguide losses[15-17].

This present approach is based on the concept of our novel frequency tripler demonstrated as shown in Fig. 2 (a) and a symmetrical monolithic integrated circuit is achieved to extend work frequency to 500 GHz in Fig. 2 (b). The novel balanced scheme, compared with the traditional power-combined tripler circuit, leaves out the on-chip capacitor and increases the power handling by a factor of two compared to the circuits in Fig. 1. To provide perfect RF and DC grounding with inherent even-order harmonics elimination, two symmetrical multiplying cells would be driven by a 180-degree power splitter and integrated on a 15 μm thick GaAs substrate as shown in Fig. 3. Compared with traditional power-combined frequency multiplier[17-19], the monolithic integrated circuits not only avoid the introduction of uncontrollable errors in the manufacturing and assembly process, but also eliminate the waveguide Y-junction, to reduce transmission losses and improve multiplication efficiency. The demonstrated tripler could handle more than 200 mW at the input, which results in a peak output power of 16 mW at 522 GHz.

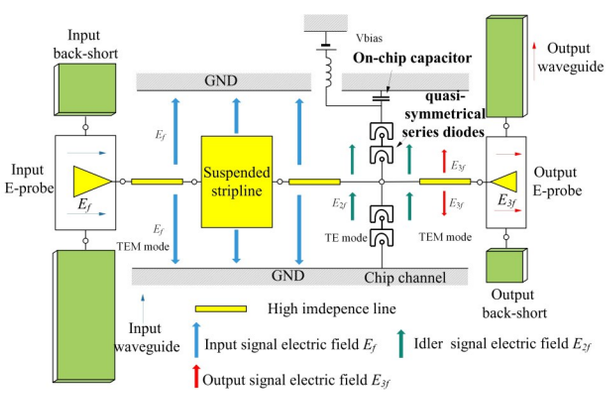
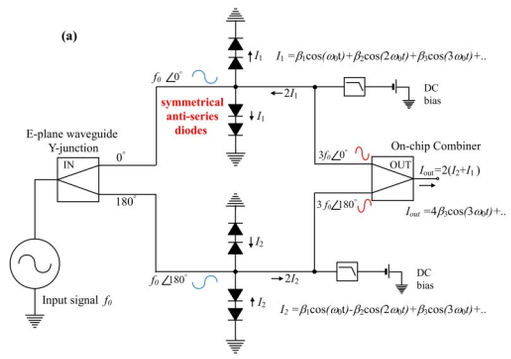


Fig. 1 Diagram of the classical balanced tripler with on-chip MIM capacitor
图1 集成MIM电容的经典平衡式三倍频器示意图

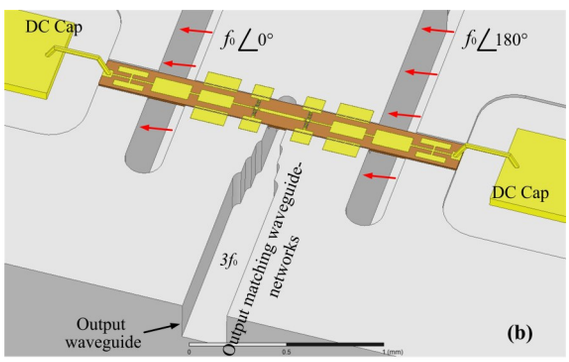
1 Tripler architecture and design

Fig. 2 (b) illustrates the basic diagram of the tripler demonstrated in this work. The input section of the circuit consists of a pair of multiplier cells which are driven by a 180-degree power splitter (E-plane Y-junction structure), leading to two intermediate outputs out-of-phase at odd order harmonics and in-phase at even order harmonics because of frequency multiplication. Currents excited under positive and negative conditions could be expressed as I1 and I2 according to Ref. [20]. An E-plane probe-based 180-degree combining structure is utilized at the output to bridges these two intermediate outputs which would eliminate the even harmonics and yield a balanced frequency tripler as a result. Thus, this topology establishes the balance and symmetry through a couple of differential input and output structures rather than a bypass capacitor required in traditional circuits.

The tripler is a split-block waveguide module that features eight Schottky planar varactor diodes and monolithically fabricated on a 15 μm-thick GaAs-based substrate with a dimension of 1938 μm×170 μm, which is sufficiently thick for thermal dissipation. Meanwhile, each tripler cell comprises four varactor diodes which are connected in anti-series at dc (shown in Fig. 3). The ba-



(a)



(b)

Fig. 2 Diagram of the proposed and novel 510 GHz tripler structure (a) tripler overall principle structure, (b) 3D view of the bottom part of the waveguide block
图2 提出来的新型510 GHz三倍频器示意图(a)三倍频器整体原理结构,(b)下部分波导腔体的三维结构图

sic strength is that in the monolithic integrated tripler, the customized diode structure and the iterative procedure are employed for improving the conversion efficiency. The first step in the customized design is to determine the zero-bias junction capacitance Cj0, the anode dimensions and the doping level of the diodes with a given input power after an iterative process. For the design of the 510 GHz tripler, to avoid the frequency shift down, a small anode size of 3.2 μm×3.2 μm is adopted and these varactors are expected to yield the zero-bias junction capacitance of 15 fF and series resistance of 8 Ω, which is in accord with the empirical rule introduced in [8]. Other electrical parameters considered in the simulations are a saturation current *I*sat=50 fA, an ideality factor n=1.2 and a junction potential V_j=0.7 V. The practical value of the reverse saturation current is difficult to predict and measure, which depends on the temperature of the junction, so it is fixed to an ideal value to simplify the design.

In addition to the electrical parameter of the Schottky diode, the three-dimension structure would influence significantly the simulated tripler performance. The 3D geometrical structure of the diode is modeled accurately in electric-magnetic simulation software. This needs to be stressed that the channel width Lslot and air-bridge width are the crucial parameters to preserve the coupling balance between the anodes. Hence, compared with the quartz-based tripler circuit based on commercial diodes[18], several iterations between a harmonic balance simulator, ADS and 3D EM simulator, HFSS would be executed to find an optimum diode structure, where the channel width and air-bridge width are optimized to maximum conversion efficiency. In the 510 GHz tripler, the channel width Lslot and air-bridge width in the diodes are designed to 8 μm and 3.2 μm.

The diode series resistance could be reduced by minimizing the epilayer thickness and increasing doped N+ layers[21]. However, the excessively short thickness of the epilayer layer would result in a lower capacitance modulation and limit the multiplier efficiency. Considering the limitation of our process, the GaAs chip is processed by a metal-organic chemical vapor deposition (MOCVD) on GaAs substrate, which consists of a 200 nm SiO_2 layer, a 300 nm N- layer with a doping concentration level of 3×1 017 cm^{-3} and a 3.5 μm N+ layer with a doping concentration level of 2×1 018 cm^{-3}, as shown in Fig. 3. The whole planar chip is inserted into the suspended channel with a cross section of 75 μm×150 μm.

The design and optimization objective in the tripler circuit is to maximize tripler efficiency with a pumping power over 200 mW available in our laboratory. It could be divided into two critical steps-1) determining details of the varactor array, such as the anode and air bridge dimensions, zero-junction capacitance as mentioned and 2) determining the proper embedding impedances to present to each junction at the internal coaxial wave ports driven under the operating frequencies (f_0=170 GHz and 3 f_0=510 GHz) based on the methodology presented in Ref. [8]. Unlike the traditional power-combined tech-

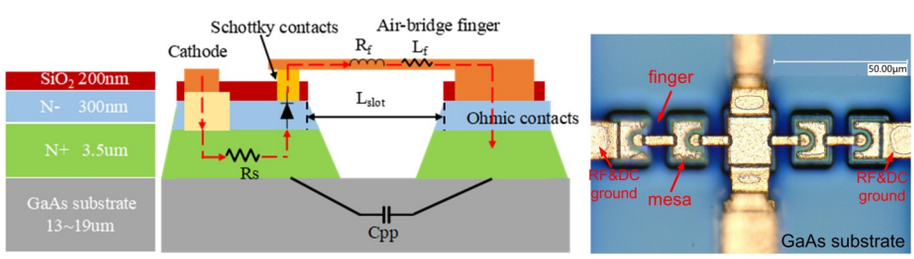


Fig. 3 The schematic cross-section and physical image of the fabricated varactors array on 15 μm thick GaAs substrate
图3 在15 μm厚的GaAs衬底上制造的二极管阵列的截面示意图和实物图像

niques based on power-combining several discrete devices[22], the proposed tripler topology could avoid imbalances bringing from the alignment of the manually assembled device or diode. What is important, it abandons the waveguide-based power combiners, such as Y-junctions or hybrid couplers, and achieve the direct and concise on-chip power-combiner. Fig. 4(a-c) shows the three main networks used to design the proposed balanced device: a) an E-plane Y-junction power splitter with simple impedances matching implemented in WR5.1 waveguide; b) a pair of tripler cells in mirror symmetry generating two intermediate outputs out-of-phase at odd harmonics; and c) a 180-degree power combining structure based on two symmetry E-plane probes achieving the differential output in the WR 1.9 band.

In this circuit, the input signals in WR5.1 waveguide would be divided into two parts with equal amplitude and opposite phase over the bandwidth through an E-plane Y-junction waveguide power splitter, which provides the critical differential inputs to the tripler pairs in mirror symmetry. The phase relations of this Y-junction structure are indicated by different arrows in Fig. 4(a).

Inside each tripler cell, an E-plane probe (integrated with dc path) located in the input waveguide couples the fundamental signals in TE_{10} mode to the suspended microstrip circuit which operating in quasi-TEM mode. This suspended network features several sections of high and low impedance which could match the varactors and prevent the high order harmonics including $2f_0$ and $3f_0$ from leaking into the input waveguide. Distributions of the electrical fields and related harmonic currents are represented by the arrows in red, as shown in Fig. 4(b). It could be seen that the directions of E-fields in these two mirror-symmetric E-probes would be totally opposite. As a result, diode pair on right side and left side would be excited under input signal with different polarity, which results in the current expressions of I_1 and I_2 respectively presented in Fig. 2(a).

The impedances and length of the suspended lines in Fig. 4(b) form the primary matching networks for the fundamental harmonic embedding impedance. The idler circuit at the second harmonic comprising the low-pass filter and virtual ground, which presents an effective short circuit to the varactors and result in purely reactive idler impedance. As for the third harmonic, the characteristic impedances and lengths of the suspended lines from the LPF to the output probe form the basic tuning elements for related embedding impedance. Based on the co-simulations of HFSS and ADS, the lengths and impedances of the suspended lines have been tuned to achieve optimized embedding impedances at each harmonic frequency range. Impedances of each harmonic might affect each other and should be optimized as a whole.

The crucial 180-degree combining structure in Fig. 4(c), compared to Y-junction combiner in common frequency tripler, provides the differential combination to those two intermediate outputs discussed above and is short electric length which facilitates to reduce propagation loss. The even order components in I_1 and I_2 would

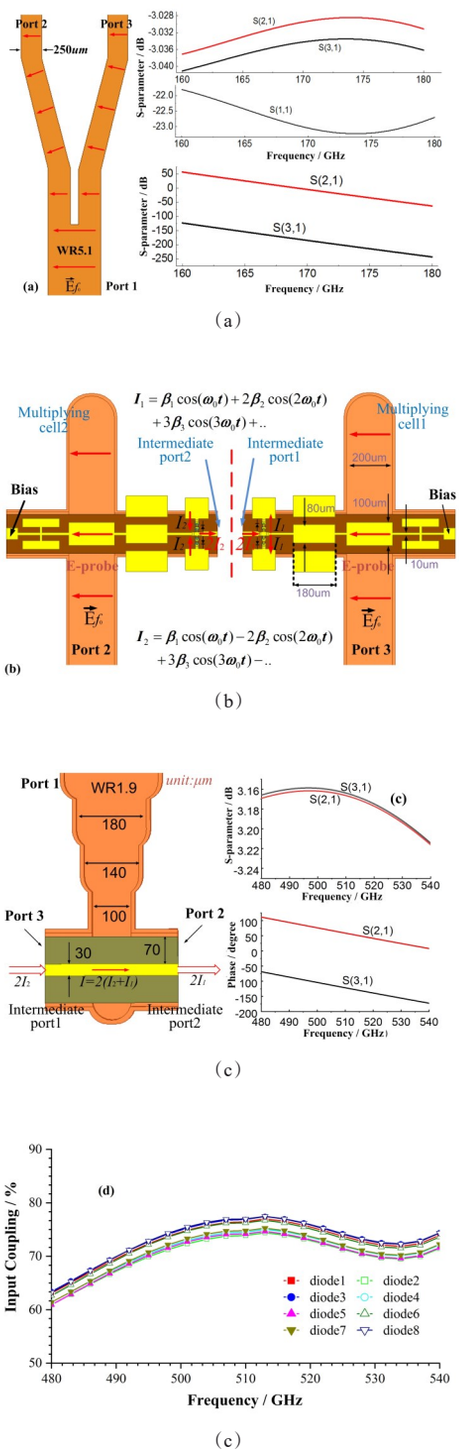


Fig. 4 Diagram and simulated result of critical sections of the tripler Note: (a) input E-plane Y-junction structure with related simulation results, (b) tripler cells in mirror symmetry with matching and filtering networks, (c) output combing structure based on E-probes with related amplitude and phase properties, (d) simulated input coupling per diode

图4 三倍频器关键结构和仿真结果 注:(a)输入E平面Y型的仿真结构,(b)镜像对称的倍频单元,(c)合成输出E面探针幅相特性,(d)每个二极管的耦合系数

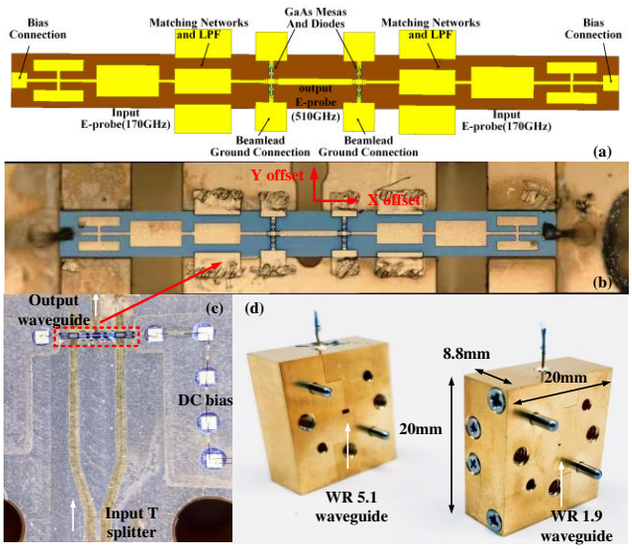


Fig. 5 Final processing structure and physical diagram of the 510 GHz tripler (a) layout of the full monolithic integrated tripler chip with a dimension of 170 μm×1938 μm×15 μm, (b) the circuit mounted on the half split-block, (c) the entire inner close-up view of tripler, (d) dimension and waveguide parameter
图 5 510 GHz 三倍频器最终加工结构与实物图 (a)尺寸为 170 μm×1 938 μm×15 μm 的整体三倍频器电路结构,(b)安装在下腔体的电路细节图,(c)倍频器完整的内部结构图,(d)三倍频器的尺寸与波导参数

be totally trapped between the low pass filters (LPF) and the virtual ground plane represented by red dotted line in Fig. 4(b). On the contrary, odd-harmonic current components in I_1 and I_2 would be combined in-phase at the output probe, where the fundamental harmonics are cut off by the WR1.9 waveguides (f_{cTE10}=311 GHz).

After the global optimization based on the above three symmetrical structures, the balance between the diodes should be analyzed to avoid the power overload in one diode. The simulated balance of input coupling presented in Fig. 4(d), is about 5% and better than traditional tripler structure[8], which owes to the symmetrical and balanced tripler structure.

Finally, Fig. 5 shows the final geometry of the fabricated tripler chip, which is approximately 170 μm×1938 μm based on the 15 μm thick Gallium Arsenide (GaAs) and comprising eight varactors with related matching networks and bias connections. Meanwhile, a fabrication error estimate is done taking into consideration the installation tolerances of the integrated circuit and a variation of 20% in the diode junction capacitance, as depicted in Fig. 6. From the result of tolerance analysis of installation and diode parameter, the horizontal X offset of installation position, DC resistance Rs and zero-bias junction Cj0 would greatly affect the frequency doubling performance and working frequency of the circuit. The horizontal offset directly breaks the symmetry of two symmetrical tripler cells, thus affecting the coupling output efficiency of signals. A variation of 20% in DC resistance induces maximum conversion efficiency to fluctuate between 7.5 and 12.5, where excess resistance converts signal energy into heat. The zero-bias junction capacitor determines the exponential nonlinearity of the diode. The smaller the capacitor is, the more suitable it is for designing high-frequency devices. Nevertheless, tiny epitaxial layer area will increase the resistance and deteriorate the double performance. Only the vertical offset has little effect on the simulation results and slightly reduces the bandwidth of the frequency doubler.

2 Fabrication and measurements

As shown in Fig. 5, the whole tripler module comprises a WR-5.1 Y-junction splitter, a pair of multiplying cells and a differential output E-probe which is easier to assemble than combination of several discrete chips in Ref. [18].

2.1 Frequency sweep

The driver chain of the 510 GHz novel balanced frequency triper is contributed by a W-band quadrupler followed by a high power amplifier with 27 dBm saturation power, a W band isolator and a 170 GHz frequency doubler presented in Fig. 7(a). Ours self-design driver power is 50~218 mW among the 163~176 GHz band as shown in Fig. 7(b). The maximum power that can be handled by the 510 GHz tripler is suggested under 200 mW based on the thermal analysis of the chip.

The outpower of 510 GHz tripler is measured using Erickson PM5 power meter and a WR1.9 to WR10 taper. The bias voltage is adjusted between -2 V to -6 V for maximum output power at each frequency. Fig. 7(c) shows that two novel 510 GHz triplers produce more than 5mW from 490 to 530 GHz with a peak power of 16 mW at 522 GHz under the 200 mW 170 GHz doubler. The conversion efficiency is among 3% to 11% in the corresponding frequency. Peak efficiency of 11% is achieved with 100 mW input power at 497 GHz. Fig. 7(c) shows an abrupt drop of output power between 505 GHz to 515 GHz. On the one hand, there is no isolator between the two multipliers and mismatch interaction to cause the disturbance of efficiency. On the other hand, the process errors of this chip structure and installation tolerances exist, such as the thickness of GaAs substrate (15~18 μm), the horizontal X offset and zero-bias junction capacitance, as the above tolerance analysis, which disturb the matching network. As show in Fig. 6(a), the horizontal offset would seriously deteriorate the flatness of doubling efficiency and zero-bias junction capacitor induce the work frequency shift. From the simulated result, when the horizontal X offset reach 20 μm, the efficiency decreases from 11% to 6% at 510 GHz and the double peak pattern forms between 500 GHz and 520 GHz, which is consistent with the measured results. To verify the effect of input power on the frequency doubling performance, Fig. 8 shows a comparison of the simulated and measured frequency doubling efficiency with input power at 505 GHz. When the input power increases from 20 mW to 210 mW, the frequency doubling efficiency is maintained between 1% and 11% and reaches the maximum values 11% at 110 mW. A similar trend exists in the measured results, but with a downward deviation. A reasonable explanation is that excessive input power

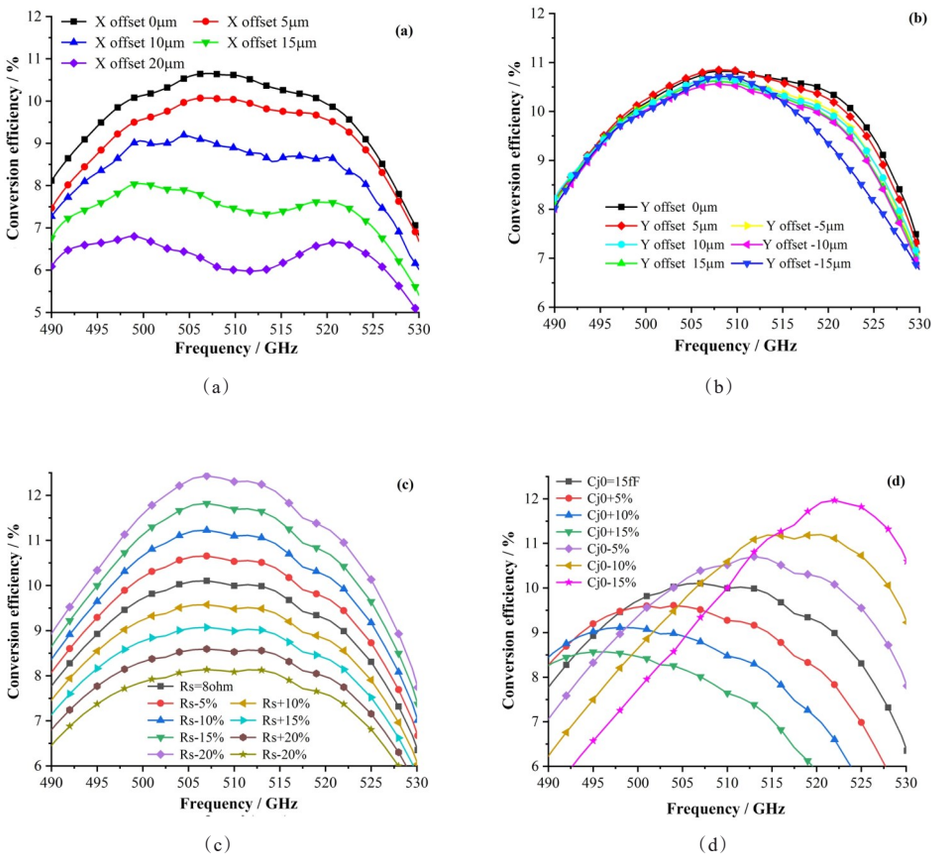


Fig. 6 Tolerance analysis of mounting positions and diode parameters Note: (a) horizontal X offset of installation position, (b) vertical Y offset of installation position, (c) +/- 20% change in DC resistance Rs, (d) +/- 15% change in zero-bias junction capacitor Cj0

图6 对安装位置和二极管参数进行公差分析 注:(a)安装位置的水平X偏移,(b)安装位置的水平Y偏移,(c)串联电阻的±20%以内的变化,(d)零偏结电容±15%以内的变化

will cause the junction temperature to rise, thus changing the parameters of the diode, such as increasing the DC resistance. When the input power increases from 100 mW to 200 mW, the multiplier efficiency decreases from 11% to 7%. In addition to the above cases, the bias voltage also has a great influence on frequency doubling performance. The output power increases from 5 mW to 13 mW when the bias voltage changes from -2 V to -6 V. The bias voltage can adjust the thickness of the depletion layer to adjust the matching characteristics of specific frequency points. In general, the optimal bias point of each frequency point needs to be fine-tuned to obtain the maximum output power.

The spectral purity of the 510 GHz frequency tripler is measured with Rohde & Schwarz FSW spectrum analyzer and Farran WR2.2 325~500 GHz frequency extension module. Due to RF power limits of extension module (-10 dBm) and lack of WR2.2 attenuator, the measured multiplier and extension module is connected with a pair of WR 2.2 diagonal horn antenna. The input frequency F0 of measured tripler is set to 165 GHz, hence, the second harmonic 2*F0 and third harmonic 3*F0 would be detected by WR2.2 frequency extension module. Fig. 9 shows the measured response at 495 GHz. The undesired second harmonic is -11.5 dB and -16.8 dB below with respect to the main third harmonic signal in the conventional ACST tripler and the proposed tripler, which confirmed that the proposed symmetrical circuit structure has greatly suppressed the second harmonic signal.

2.2 Comparison

The performance of the proposed symmetrical and balanced 510 GHz is compared with previously research. In this frequency range, the conversion efficiency of the proposed tripler is higher than Ref. [21] under 100 mW input power, though output peak power is relatively low. In the future, the GaAs diode in the circuit would be substituted by the one with higher reverse breakdown voltage and larger anode size, and the number of diode in tripler cells increase from four to six, to enhance handing power capacity and peak output power. Compared with conventional design of tripler, the proposed scheme has built the perfect balance structure without on-chip capacitor, and avoids the unnecessary transmission loss by reducing the electrical length in output waveguide. The alignment and symmetry of the tripler circuits could be easy to preserve during fabrication and assembling.

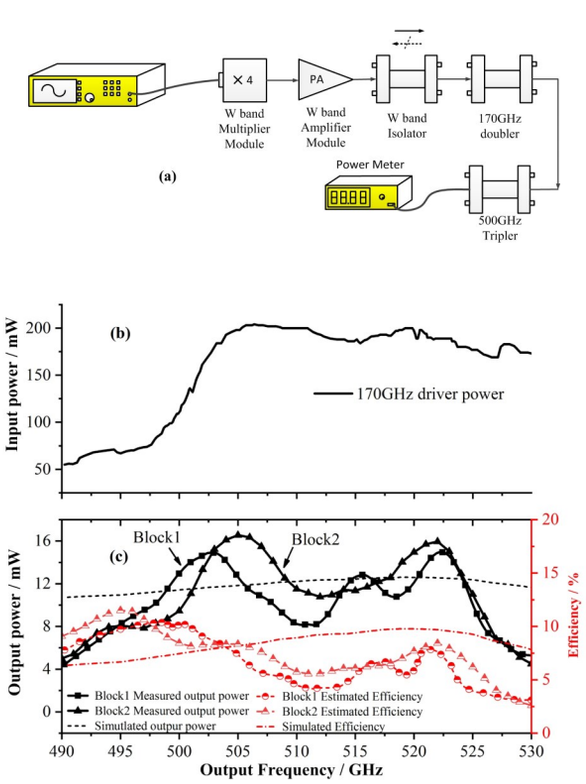


Fig. 7 The measured result of 510 GHz tripler (a) test setup for the 490-530 GHz tripler, (b) available 170 GHz doubler output power, (c) the measured output and conversion efficiency as a function of output frequency

图 7 510 GHz 三倍频器测试结果 (a)490~530 GHz 三倍频器测试平台,(b)可用的 170 GHz 倍频器输出功率,(c)实测输出功率与倍频效率随输出频率的变化

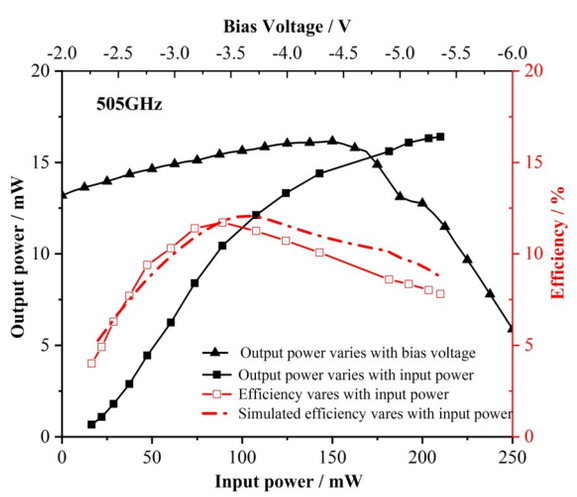


Fig. 8 The output power of the tripler at 505 GHz varies with bias voltage, input power

图 8 三倍频器的输出功率在 505 GHz 处随偏置电压和输入功率的变化

3 Conclusions

A high-power terahertz Schottky diode based symmetrical tripler configuration at 500 GHz is reported which uses 180-degree power splitter in input and a pair of symmetrical tripler in output to enhance the power handing. The peak conversion efficiency and maximum output power of 11% and 16 mW is presented. The scheme of tripler offers an important option to build more powerful and pure sources at terahertz frequency. This 510 GHz multiplied sources would be served as the local oscillator of a 1 THz heterodyne receiver.

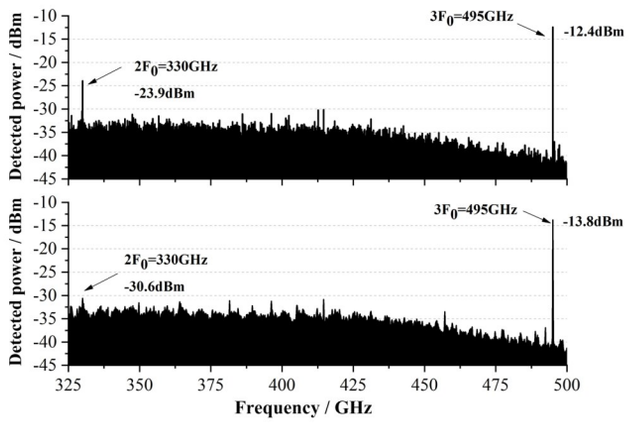


Fig. 9 The spectrum result of the 495 GHz signal produced by tripler (a) the conventional ACST tripler, (b) the proposed tripler

图 9 由三倍频器产生的 495 GHz 频率特性 (a)ACST 三倍频器,(b)本文提出的三倍器

Table 1 Performance comparison of millimeter frequency triplers

表 1 毫米波三倍频器性能对比

Ref	On-chip Capacitor	Number of diode	Balanced or not	Freq/ GHz	Peak power / mW	Efficiency / %
[8]	yes	6	yes	540-640	1.55	4.5-9
[11]	yes	8	yes	840-900	1.46	1-3
[15]	yes	12	yes	265-330	24	5-15
[21]	yes	12	yes	510-552	35	~7
[23]	yes	12	yes	210-225	45	3-15
This Work	**no**	**8**	**yes**	**490-530**	**16**	**3-11**

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