第37卷第3期 红外与毫米波学报 Vol. 37, No. 3
2018年6月 J. Infrared Millim. Waves June, 2018

文章编号: 1001-9014(2018)03-0257-05 DOI: 10.11972/j.issn.1001-9014.2018.03.001

Digital output for short-wave infrared InGaAs linear FPA

WEI Yang[1,2,3,4], WANG Xu-Quan[1,2], HUANG Zhang-Cheng[1,2], HUANG Song-Lei[1,2*], FANG Jia-Xiong[1,2*]

(1. State Key Laboratories of Transducer Technology, Shanghai Institute of Technical Physics, Chinese Academy of Science, Shanghai 200083, China;
2. Key Laboratory of Infrared Imaging Materials and Detectors, Shanghai Institute of Technical Physics, Chinese Academy of Science, Shanghai 200083, China;
3. University of Chinese Academy of Sciences, Beijing 100049, China;
4. Shanghai Tech University, Shanghai 200083, China)

Abstract: A specific digital output research on short-wave infrared InGaAs linear focal plane array (FPA) was reported. Coupled with a laboratory self-designed short-wave infrared 256 × 1 InGaAs FPA, a successive approximation register (SAR) analog to digital convertor (ADC) with high resolution, low power consumption and small size was designed and fabricated in 0.18 μm CMOS process. The chip consumes 460 μW at a sampling rate of 235 KS/s with the power supply of 3.3 V. The signal to noise ratio (SNR) of the ADC chip is 66.6 dB. The ADC chip was also tested at different integral time to convert the 256 × 1 InGaAs FPA signal. The results show that the ADC chip can meet the application requirements of the 256 × 1 InGaAs FPA.

Key words: short-wave infrared, 256 × 1 InGaAs FPA, ADC, successive approximation register SAR
PACS: 07.57.kp

短波红外 InGaAs 线性焦平面数字化输出研究

魏 杨[1,2,3,4], 王绪泉[1,2], 黄张成[1,2], 黄松垒[1,2*], 方家熊[1,2*]

(1. 中国科学院上海技术物理研究所 传感技术联合国家重点实验室,上海 200083;
2 中国科学院上海技术物理研究所 中国科学院红外成像材料与器件重点实验室,上海 200083;
3. 中国科学院大学,北京 100049;
4. 上海科技大学,上海 200083)

摘要: 提出了一种适用于短波红外铟镓砷线性焦平面的数字化输出研究. 针对实验室自主研制出的短波红外256 × 1 铟镓砷焦平面,结合 SAR ADC 的基本原理,以高分辨率、低功耗、小面积为设计原则,设计一款逐次逼近(SAR)模数转换器. ADC 采用0.18 μm CMOS 工艺流片,采用3.3 V 电压供电,采样率235 KS/s,功耗460 μW,信噪比66.6 dB. 将 ADC 芯片与256 × 1 铟镓砷焦平面在变积分时间条件下进行耦合测试. 结果表明 ADC 芯片可以满足短波红外线列256 × 1 铟镓砷焦平面的应用需求.

关 键 词: 短波红外; 线列256 × 1 铟镓砷焦平面; 模数转化器; 逐次逼近

中图分类号: TN402 **文献标识码:** A

Introduction

Short wave infrared InGaAs focal plane array (FPA) has a high responsivity in the short wave infrared band (typical 0.9 ~ 1.7 μm), and is widely used in spectral analysis and real-time imaging. Several typical 256 × 1, 512 × 1, 1024 × 1, 320 × 256 and 640 × 512 InGaAs FPAs with analog output were equipped in short-wave infrared spectrometers and cameras [1]. As a core component of micro spectrometer and cameras in this band, InGaAs FPAs are developing towards small size,

Received date: 2017-10-10, **revised date:** 2018-03-04 **收稿日期:** 2017-10-10, **修回日期:** 2018-03-04
Foundation items: Supported by the National Key R&D Program of China (2016YFB0402401) and the National Science Foundation of China (61376052, 61475179 and 61604159)
Biography: WEI Yang (1991-), male, Wuhan, PhD student. Research area involves Microelectronics and Solid State Electronics. E-mail: weiy@mial.sitp.ac.cn
* **Corresponding author:** E-mail: huangsl@mail.sitp.ac.cn, fangjx@mail.sitp.ac.cn

light weight and low power consumption (SWaP). Under this trend, increasing attentions are paid to developing digital FPAs to replace traditional analog FPAs, and challenging works are focused on analog to digital convertors (ADC) [2]. Since reducing the FPA noise is considered as the primary task [3], ultra-low noise design is needed to be considered for a good matching with such FPAs. Furthermore, the power consumption and small chip area are also important. With the development of FPA, the digital InGaAs FPA will be of great concern. At present, there are several studies on the focal plane digitalization. An 8 × 1 InGaAs FPA with 10-bit SAR ADC was designed in Refs. [4-5], which proposed an output scheme for 512 × 512 FPA using 12-bit SAR structure.

In this paper, a 14-bit 235 KS/s successive approximation register (SAR) ADC in 0.18 μm CMOS process is described for the specific 256 × 1 InGaAs FPA application. The research object is a laboratory self-designed short-wave infrared InGaAs micro spectrometer, which is implemented with a 256 × 1 InGaAs focal plane as the core components.

1 Architecture

The eclectic scheme is shown in Fig. 1. An ADC chip was fabricated to replace the ADC device which is widely used in conventional scheme. The analog output signal of InGaAs FPA is directly converted by the ADC chip which could reduce the system complexity and simplify the analog signal channel.

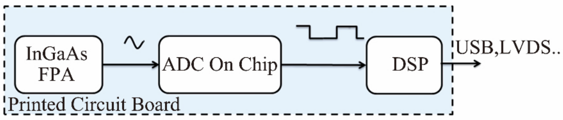

Fig. 1 The proposed digital scheme of InGaAs FPA output
图 1 一种铟镓砷焦平面数字输出方案

The 256 × 1 InGaAs FPA has two signal-ended outputs applied with correlated double sampling (CDS) technique [6]. This can result in a significant problem of the interface uniformity between FPA and ADC. If a full differential input mode of ADC is chosen, a high performance single-ended to differential converter is needed, and thus the power consumption and chip area is increased as well. What is worse, the noise of such a single-ended to differential converter followed by an amplifier can be multiplied, decreasing the performance of the ADC. To solve this problem, a pseudo differential input mode is used, which can also decrease the power consumption and chip area caused by the single-ended to differential converter. In addition, the ADC resolution is limited to 12 bits, as a result of a commonly-used dynamic comparator [7]. This is not suitable to advanced digital FPAs. Hence, a conventional statistics comparator is applied to enhance the resolution.

Figure 2 shows the block diagram of the proposed ADC. It comprises a 14-bit matched binary-weighted charge redistribution DAC with switching array, a high precision comparator with two stage output offset storage

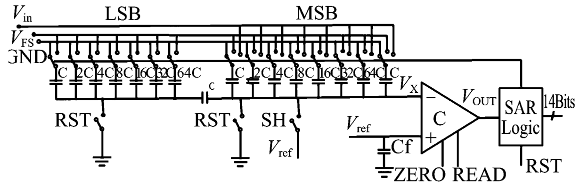

Fig. 2 Architecture of the proposed SAR ADC
图 2 采用的逐次逼近架构模数转换器结构

technique, and a synchronous SAR logic. In addition, a decoupling compactor is added at the reference voltage to minimize the interference. To reduce the total capacitance, the 14-bit charge redistribution DAC with split structure is used.

During the sampling time, MSB capacitors participate in the sampling while LSB capacitors remain to ground. Two switches are added at the top-plate nodes of MSB and LSB capacitors to keep the attenuating capacitor with no charge injection during the reset time. Meanwhile, the bottom-plate nodes of all binary weighted capacitors are connected to ground to make sure the whole capacitor array with no charge storage.

2 Circuit implementation

In this section, the circuit level design of 14-bit charge redistribution DAC and high precision comparator are described.

2.1 Charge redistribution DAC

The unit capacitor is used to reduce the mismatch with the capacitor array. Normally, the relationship between total capacitance and DAC resolution is given by Eq. (1). In fact, given that a split structure is used, the relationship should be presented by Eq. (2). The great reduction of the total capacitance can reduce ADC power consumption and the overall ADC size. The voltage of node V_X shown in Fig. 2, which is directly connected to the inverting input of comparator, is given by Eq. (3) in the design.

$$C_{Total} = 2^N \cdot C_{Unit} \quad , \quad (1)$$

$$C_{Total} = 2^{N/2} \cdot C_{Unit} \quad , \quad (2)$$

$$V_X = \frac{128C}{128C(127C//C)} \cdot \left(-V_{in} + \sum_{i=1}^{14} \frac{b_i}{2^{15-i}} V_{ref}\right) + V_X \quad . \quad (3)$$

The unit capacitor has a great impact on the power consumption and noise of the DAC. In general, the unit capacitance should be designed as small as possible to reduce the power consumption. However, the smaller the value of unit capacitor, the larger KT/C noise of the whole capacitive DAC [9]. Its relationship can be given by Eqs. (4) [10] and (5). A relative balance is to take account into the design in order to grantee the power saving and low noise. The unit capacitance C is set 40 fF, which makes the KT/C lower than the quantization noise and saves the power consumption at an acceptable level. Hence, the sampling capacitance is 5 pF, and the total capacitance is 10 pF.

$$E_{Conv} = \sum_{i=1}^{n} 2^{n-2-i}(2^i - 1) C V_{FS}^2 \quad , \quad (4)$$

$$\frac{2K_B T}{C_{sh}} \leqslant \frac{1}{2} \cdot \frac{LSB^2}{12} \quad , \quad (5)$$

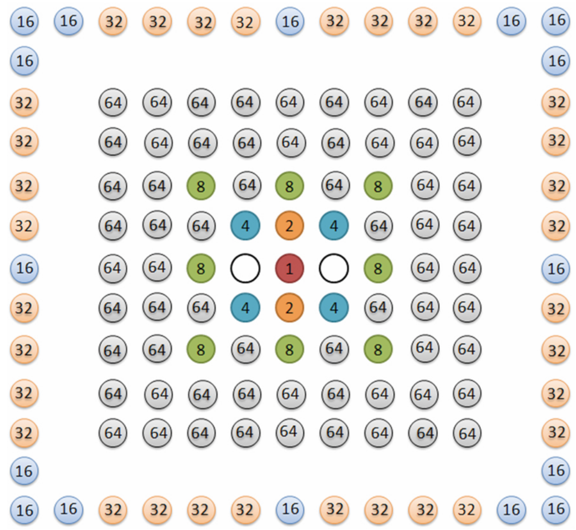

Fig. 3 A centrosymmetric distribution scheme of capacitor layout

图 3 一种中心对称分布的电容版图设计方案

In terms of the layout design, a centrosymmetric distribution scheme shown in Fig. 3 is applied to reduce the impact of capacitor mismatch. Also, some redundant capacitors are added to keep the structure fully centrosymmetric.

2.2 Comparator

The proposed comparator is implemented with a three-stage pre-amplifier, a two-stage output offset storage capacitors, a dynamic latch and an output stage, which is shown in Fig. 4. The three-stage pre-amplifier can amplify the small voltage to a large level which can be recognized by the followed by dynamic latch. This dynamic latch could increase the speed of the comparator, and the comparator is designed to satisfy the speed and accuracy requirements of ADC.

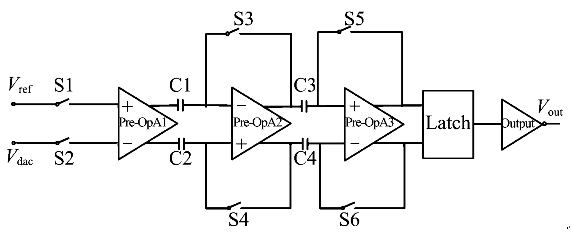

Fig. 4 Architecture of the proposed comparator

图 4 采用的比较器结构

The Output Offset Storage (OOS) technique [11] is utilized to calibrate the offset of the comparator at the beginning of each comparison. After the calibration, the offset can be reduced to Eq. (6).

$$V_{OSI} = \frac{V_{OS2}}{A_1 A_2} + \frac{V_{OS3}}{A_1 A_2 A_3} + \frac{V_{Latch}}{A_1 A_2 A_3} + \frac{\Delta q_1}{A_1 C} + \frac{\Delta q_2}{A_1 A_2 C} \quad , \quad (6)$$

where V_{OS1}, V_{OS2}, V_{OS3} and V_{LATCH} represent the offset of pre-amplifiers 1, 2 and 3, respectively, and Latch. A_1, A_2 and A_3 represent the gain of pre-amplifiers 1, 2 and 3, respectively, and $\triangle q_1$ and $\triangle q_2$ represent the stored charge of capacitors 1, 2 and capacitors 3, 4, respectively, and C is the capacitance of each capacitor.

3 Measurement results

In this section, the test results of ADC performance are described in Sect. 3.1, and comparison result of ADC applied to 256 × 1 InGaAs FPA is shown in Sect. 3.2.

3.1 ADC performance

The prototype SAR ADC with a core area of 1 344 × 538 μm^2 was designed and fabricated in 0.18 μm One Poly Six Metal (1P6M) CMOS process. It was packaged in a 1.27 mm pitch Dual Inline Pin (DIP) package. In FPA applications, the noise of ADC should not be larger than the noise of FPA. Hence, the most-concerned performance of ADC is SNR. The noise of 256 × 1 InGaAs FPA changes from 0.4 to 1 mV, which is related to the integral time. Figure 6 shows the SNR of different input signal from 0 to 2 V. As we can see, the SNR of ADC is 66.6 dB, which means the ADC noise is about 0.33 mV. Thus, the ADC proposed can be perfectly used in 256 × 1 InGaAs FPA. Other performance is list in Table 1.

Table 1 ADC performance summary

表 1 ADC 性能参数汇总

Technology	0.18 μm CMOS
Sampling Rate	235 KS/s
Die Area	1 344 × 538 μm^2
Power Consumption	460 μW
Differential Nonlinearity (DNL)	−2 LSB /1 LSB
SNR	66.6 dB
Effective Number of Bits (ENOB)	10.8
Input Range	0 ~ 2 V
Quantization Noise	0.33 mV

Figure 5 shows the simulation and measurement SNR results of ADC chip in different input signals. The simulation result (black dots) shows that the SNR is 71.5 dB. Thus, the ENOB is 11.5 bits and quantization noise is 0.19 mV. The measurement results (red dot) show that the SNR is 66.6 dB, which means the ENOB is 10.8 bits and quantization noise is 0.33 mV. The deviations between simulation and measured result may be caused by the circuit manufacturing process and test source jitter.

3.2 Comparison result between ADC and data acquisition card

Generally, data acquisition card is used to convert analog outputs to digital code in traditional 256 × 1 InGaAs FPA tests. Series of output data in different integral time of 256 × 1 InGaAs FPA were acquired by data acquisition card. By contrast, ADC chip can converter the analog outputs of InGaAs FPA. Figure 6 shows the test equipment. The blackbody at 900 K is the radiation source to irradiate the detector. The 256 × 1 InGaAs FPA turns the light signal into analog voltage signal. Then,

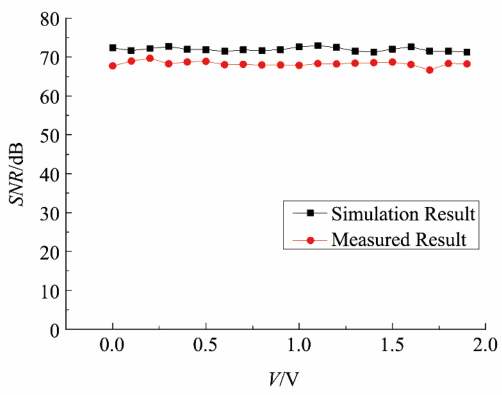

Fig. 5 Simulation and measured SNR results of ADC chip in different input signals
图5 不同输入信号下,仿真和测试得到的 ADC 芯片的 SNR 值

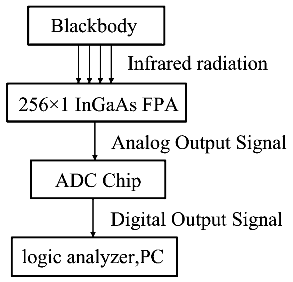

Fig. 6 Flowchart of the proposed 256 × 1 InGaAs FPA testing scheme with digital output
图6 采用数字化输出的 256 × 1 铟镓砷焦平面测试方案示意图

the proposed ADC chip converts this analog voltage signal into digital code. Finally, the logic analyzer recognizes the digital code and transfers them to the computer.

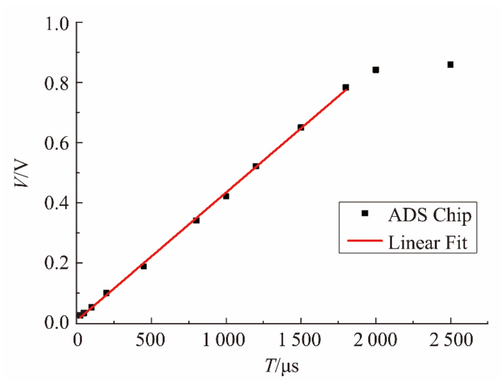

Fig. 7 The 256 × 1 InGaAs FPA output signal by the proposed ADC chip
图7 ADC 芯片转换的 256 × 1 铟镓砷焦平面输出信号结果

In this experiment, the distance from blackbody to the FPA was 30 cm. The FPA was tested under different integral time. The integral time ranges from 10 μs to 2 500 μs, because more or less than this could make signal weak or saturated. The converting performance is most-concerned. Figure7 shows the comparison result. From 10 μs to 1 800 μs, the FPA output signal increases linearly with the integral time. The first order interpolation coefficient of these dots is 99.9%. After 1 800 μs, the FPA output signal tends to saturation. Increasing the distance from blackbody to FPA or decreasing the blackbody aperture can extend the linear region of FPA, while the performance remains the same.

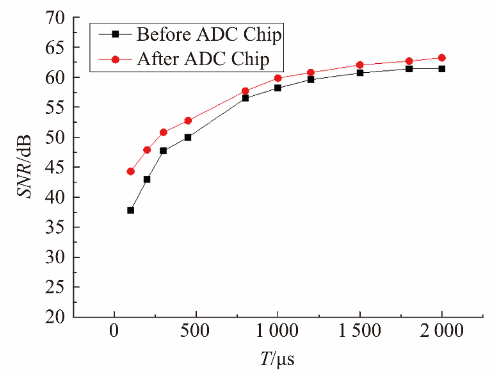

Fig. 8 Comparison result of 256 × 1 InGaAs FPA SNR with digital output and analog output
图8 数字输出和模拟输出 256 × 1 铟镓砷焦平面信噪比对比结果

Figure 8 shows anther result of 256 × 1 InGaAs FPA SNR with digital output and analog output. The linear region of FPA, where covers from 200 to 1 800 μs in the same test condition with output voltage measurements in Fig. 7, is concerned. The output curves of the proposed ADC chip (red circle dots) and without ADC chip (black square dots) are also shown. The minimum deviation between them is 1.4 dB, which means the digital output FPA can improve anti-jamming ability and enhance the SNR.

4 Conclusion

This paper presents a specific digital scheme suitable for shortwave infrared micro spectrometers. This design is mainly applied to the SWIR 256 × 1 InGaAs FPA developed by our own laboratory. A pseudo differential input mode has been employed in the design to meet the demands of high resolution, low power consumption and small size. The proposed SAR ADC chip was fabricated in 0.18 μm CMOS process with the core area of 1344 × 538 μm^2. The maximum sampling rate of ADC reaches at 235 KS/s. According to the comparison results between ADCs and data acquisition card, the ADC chip can meet the SWIR 256 × 1 InGaAs FPA application requirements.

Acknowledgements

The authors are grateful to many colleagues for providing InGaAs detectors and packaging for this paper.

(下转第268页)

[6] Degerli Y, Lavernhe F, Magnan P, *et al*. Non-stationary noise responses of some fully differential on-chip readout circuits suitable for CMOS image sensors [J]. *IEEE Transactions on Circuits & Systems II Analog & Digital Signal Processing*, 1999, **46**(12): 1461-1474.

[7] Dupont B, Dupret A, Belhaire E, *et al*. FPN Sources in Bolometric Infrared Detectors [J]. *IEEE Sensors Journal*, 2009, **9**(8): 944-952.

[8] Vatteroni M, Covi D, Sartori A. A linear-logarithmic CMOS pixel for high dynamic range behavior with fixed-pattern-noise correction and tunable responsivity [C]. *IEEE SENSORS* 2008 *Conference*, 2008, 930-933.

[9] Kim Y S, Woo D H, Jo Y M, *et al*. Low-Noise and Wide-Dynamic-Range ROIC With a Self-Selected Capacitor for SWIR Focal Plane Arrays [J]. *IEEE Sensors Journal*, 2017, **17**(1), 179-184.

[10] Yonemoto K, Sumi H, Suzuki R, *et al*. A CMOS image sensor with a simple FPN-reduction technology and a hole accumulated diode [C]. *Solid-State Circuits Conference*, 2000, 102-103.

[11] Wolf A, Pezoa J E, Figueroa M. Modeling and Compensating Temperature-Dependent Non-Uniformity Noise in IR Microbolometer Cameras [J]. *Sensors*, 2016, **16**(7): 1121.

[12] Cruz C A D M, Monteiro D W D L, Souza A K P, *et al*. Voltage Mode FPN Calibration in the Logarithmic CMOS Imager [J]. *IEEE Transactions on Electron Devices*, 2015, **62**(8): 2528-2534.

[13] Dem'yanenko M A, Kozlov A I, Marchishin I V *et al*. Development of analog-digital readout integrated circuits for infrared focal plane arrays [J]. *Optoelectron. Instrument. Proc*, 2016, **52**(6): 630-636.

[14] Woo D H, Nam I K, Lee H C. Smart Reset Control for Wide-Dynamic-Range LWIR FPAs [J]. *IEEE Sensors Journal*, 2011, **11**(1): 131-136.

[15] Im S, Park S G. Thermal noise analysis of switched-capacitor integrators with correlated double sampling [J]. *International Journal of Circuit Theory & Applications*, 2016, **44**(12): 2101-2113.

[16] Popowicz A. Analysis of correlated double sampling circuit with integration [J]. *Przeglad Elektrotechniczny*, 2012, **88**(2): 200-203.

[17] Altun O, Tasdemir F. Low-noise readout circuit for SWIR focal plane arrays [C]. *SPIE Defense + Security*, 2017: 1017707.

[18] Enz C C and Temes G C. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization [J]. *Proceedings of the IEEE*, 1996, **84**(11): 1584-1614.

[19] Wey H, Guggenbuhl W. Noise transfer characteristics of a correlated double sampling circuit [J]. *IEEE Transactions on Circuits & Systems*, 1986, **33**(10): 1028-1030.

[20] Kim D, Bae J, Song M. A high speed CMOS image sensor with a novel digital correlated double sampling and a differential difference amplifier [J]. *Sensors*, 2015, **15**(3): 5081-5095.

[21] Fieque B, Tissot J L, Trouilleau C. Uncooled microbolometer detector: Recent developments at Ulis [J]. *INFRARED PHYSICS & TECHNOLOGY*, 2007, **49**(3): 187-191.

[22] Kim G, Lim S, Kim Y, *et al*. High-uniformity post-CMOS uncooled microbolometer focal plane array integrated with active matrix circuit [C]. *Transducers & Eurosensors Xxvii: the, International Conference on Solid-State Sensors, Actuators and Microsystems. IEEE*, 2013: 2361-2364.

(上接第 260 页)

And the project is supported by National Key R&D Program of China (2016YFB0402401) and the National Science Foundation of China (No. 61376052, 61475179 and 61604159).

References

[1] SHAO Xiu-mei, GONG Hai-mei, LI Xue, *et al*. Developments of High Performance Short-wave Infrared InGaAs Focal Plane Detectors [J]. *Infrared Technology*, 2016, **38**: 629-635.

[2] Omer Ceylan, Atia Shafique, Abdurrahman Burak, *et al*. Digital readout integrated circuit (DROIC) implementing time delay and integration (TDI) for scanning type infrared focal plane arrays (IRFPAs) [J]. *Infrared Physics & Technology*, 2016, **79**: 101-112.

[3] HUANG Zhang-cheng, CHEN Yu, HUANG Song-lei, *et al*. Analysis and simulation of a new kind of noise at the input stage of infrared focal plane array [C]. *Proc. SPIE*, 2014. **9100**(3).

[4] ZHU Hui, LI Yao-qiao, CHEN Xin-yu, *et al*. A design scheme of digital output for IRFPA [J]. *Laser & Infrared*, 2007, **37**: 997-1000.

[5] GAO Lei, ZHAI Yong-cheng, LIANG Qing-hua, *et al*. RFPA ROIC integrated digital output [J]. *InInfrared and Laser Engineering*, 2015, **44**(6): 1686-1691.

[6] HUANG Song-lei, HUANG Zhang-cheng, CHEN Yu, *et al*. A low noise high readout speed 512 × 128 ROIC for shortwave InGaAs FPA [C]. *Proc. SPIE*, 2015, 9521.

[7] Gisela de La Fuente-Cortes, Guillermo Espinosa Flores-Verdad, Victor R. Gonzalez-Diaz, *et al*. A new CMOS comparator robust to process and temperature variations for SAR ADC converters [J]. *Analog Integrated Circuits and Signal Processing*, 2017, **90**: 301-308.

[8] HUA Fan. Effective method to improve linearity of high-resolution SAR ADC [J]. *Microelectronics Journal*, 2017, **61**: 35-42.

[9] ZHANG Dai, Ameya Bhide and Atila Alvandpour. A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-m CMOS for Medical Implant Devices [J]. *IEEE J. Solid-State Circuits*, 2012, **47**(7): 1585-1593.

[10] LIU C-C, CHANG S-J, HUANG G-Y, *et al*. A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure [J]. *IEEE J. Solid-State Circuits*, 2010, **45**(4): 731-740.

[11] Phillip E. Allen, Douglas R. Holberg. CMOS Analog Circuit Design [M], Beijing: Publishing House of Electronics Industry (Phillip E. Allen, Douglas R. Holberg. CMOS 模拟集成电路设计, 北京: 电子工业出版社), 2007: 483-485.