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# High-frequency InAlN/GaN HFET with an $f_T$ of 350 GHz

FU Xing-Chang[1,3], LV Yuan-Jie[2], ZHANG Li-Jiang[1,3], ZHANG Tong[1*], LI Xian-Jie[3], SONG Xu-Bo[3], ZHANG Zhi-Rong[3], FANG Yu-Long[2], FENG Zhi-Hong[2*]

(1. Joint International Research Laboratory of Information Display and Visualization, School of Electronic Science and Engineeing, Southeast University, Nanjing, 210096, China;
2. National Key Laboratory of Application Specific Integrated Circuit (ASIC), Shijiazhuang, 050051, China;
3. Hebei Semiconductor Research Institute, Shijiazhuang, 050051, China)

**Abstract**: Scaled InAlN/GaN heterostructure field-effect transistors (HFETs) with high unity current gain cut-off frequency ($f_T$) were realized by employing nonalloyed regrown $n^+$-GaN Ohmic contacts, in which the source-to-drain distance ($L_{sd}$) was scaled to 600 nm. By processing optimization of dry etching and $n^+$-GaN regrowth, a low total Ohmic resistance of 0.16 Ω·mm is obtained, which is a recorded value regrown by metal organic chemical vapor deposition (MOCVD). A 34 nm rectangular gate was fabricated by self-aligned-gate technology. The electrical characteristics of the devices, especially for the RF characteristics, were improved greatly after the reduction of ohmic resistance and gate length. The fabricated InAlN/GaN HFETs show a low on resistance ($R_{on}$) of 0.41 Ω·mm and a high drain saturation current density of 2.14 A/mm at $V_{gs}$ = 1 V. Most of all, the device shows a high $f_T$ of 350 GHz, which is a recorded result reported for GaN-based HFETs in domestic.

**Key words**: InAlN/GaN, HFET, current gain cut-off frequency, nonalloyed Ohmic contacts, nano-gate
**PACS**: 85.30.De, 71.55.Eq, 85.30.Tv, 78.55.Cr

# $f_T$ 为 350 GHz 的 InAlN/GaN HFET 高频器件研究

付兴昌[1,3], 吕元杰[2], 张力江[1,3], 张 彤[1*], 李献杰[3], 宋旭波[3], 张志荣[3], 房玉龙[2], 冯志红[2*]

(1. 信息显示与可视化国际合作联合实验室,电子科学与工程学院,东南大学,江苏 南京 210096;
2. 专用集成电路国家级重点实验室,河北 石家庄 050051;
3. 河北半导体研究所,河北 石家庄 050051)

**摘要**:采用再生长 $n^+$ GaN 非合金欧姆接触工艺研制了具有高电流增益截止频率($f_T$)的 InAlN/GaN 异质结场效应晶体管(HFETs),器件尺寸得到有效缩小,源漏间距减小至600 nm. 通过优化干法刻蚀和 $n^+$ GaN 外延工艺,欧姆接触总电阻值达到0.16 Ω·mm,该值为目前金属有机化学气相沉积(MOCVD)方法制备的最低值. 采用自对准电子束曝光工艺实现34 nm 直栅. 器件尺寸的缩小以及欧姆接触的改善,器件电学特性,尤其是射频特性得到大幅提升. 器件的开态电阻($R_{on}$)仅为0.41 Ω·mm,栅压1 V 下,漏源饱和电流达到2.14 A/mm. 此外,器件的电流增益截止频率($f_T$)达到350 GHz,该值为目前 GaN 基 HFET 器件国内报道最高值.

**关 键 词**:铟铝氮氮化镓异质结;异质结场效应晶体管;电流增益截止频率;非合金欧姆接触工艺;纳米栅

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## Introduction

Attributed to the excellent characteristics of nitride material, *i. e.*, unique high electron velocity and breakdown electric field, AlGaN/GaN heterostructure field-effect transistors (HFETs) have shown great advantages in high-power and high-voltage applications[1]. Since the

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**Biography**:FU Xing-Chang (1975-), male, Shandong, China, Ph. D Candidate. Research fields focus on RF Microwave electronic devices. E-mail: Pasf365@163.com
* **Corresponding author**:E-mail: tzhang@seu.edu.cn, ga917vv@163.com

AlGaN barrier layer is necessary to be thick enough to generate two-dimensional electron gas (2DEG) at the interface of AlGaN/GaN, the transistor will suffer serious short channel effects (SCEs) as device scaling. Moreover, the gate modulation efficiency may also degenerate induced by the interface defects and traps. Nowadays, the recorded maximum oscillation frequency ($f_{max}$) and unity current gain cut-off frequency ($f_T$) of AlGaN/GaN HFETs are just 300 GHz and 225 GHz[2-3], respectively, limiting the applications in power amplifiers above W-band.

Due to the strong spontaneous polarization, ultrathin In(Al)N/GaN heterostructures have high 2DEG density with only several-nanometer thin barrier layer, which can overcome above challenges and achieve higher frequency[4]. The recorded values of $f_T$ and $f_{max}$ are realized based on ultrathin AlN/GaN heterostructure by scaling device[5]. However, the reliability of AlN/GaN HFETs has not been investigated, in which strong piezoelectric polarization exists. The lattice-matched InAlN/GaN heterostructures have no piezoelectric polarization, which can reduce defects resulted from the lattice mismatch and offer better reliability. Our recent research shows that the median time to failure (MTTF) of InAlN/GaN HFETs is estimated to be $8.9 \times 10^6$ hours at junction temperature of 150℃[6], indicating that InAlN/GaN HFETs can be used in future practical applications.

Outstanding advance in the frequency characteristics of InAlN/GaN HFETs has been obtained due to the improvements of device processing in recent years. A 10-nm InAlN barrier was used by Sun, *et al.*, and a combined $f_T/f_{max}$ of 205/191 GHz InAlN/GaN HFET was fabricated with 55-nm gate length[7]. Using the treatment of oxygen plasma to reduce the RF transconductance ($g_m$) dissociation, Lee, *et al.* reported a 30-nm-gate InAlN/GaN HFET with high $f_T$ of 245 GHz[8]. InGaN back barrier was introduced to suppress the SCEs, the same group achieved high $f_T$ of 300 GHz with 30-nm gate length[9]. Yue, *et al.* reported an ultrascaled InAlN/GaN HFET having a record $f_T$ of 400 GHz, in which the drain-to-source distance was reduced to 270 nm and gate length was 30 nm[10]. Our group have also done some work on the high-frequency InAlN/GaN HFETs. A 70-nm T-shaped InAlN/GaN HFET was fabricated with $f_T/f_{max}$ of 170/210 GHz using nonalloyed regrown $n^+$-GaN Ohmic contacts[11]. Besides, InAlN/GaN HFET with $f_T$ of 220 GHz was also reported with 50 nm rectangular gate[12].

In this letter, nonalloyed regrown $n^+$-GaN ohmic contacts are used in the fabrication of InAlN/GaN HFETs, in which the virtual source-to-drain distance is reduced to 600 nm. By improving the processing of dry etching and regrowth of $n^+$ GaN, the resistance of nonalloyed Ohmic contact is reduced greatly. Moreover, using self-aligned e-beam lithography, a 34 nm rectangular gate is formed in the center of the drain-to-source space. Due to the improvement of Ohmic resistance and device scaling, the fabricated InAlN/GaN HFETs show a low on resistance ($R_{on}$) of 0.41 Ω·mm, and the high drain saturation current density reaches to 2.14 A/mm at $V_{gs} = 1$ V. Most of all, the device with 34-nm rectangular gate shows a high $f_T$ of 350 GHz, which is a recorded result reported for GaN-based HFETs in domestic.

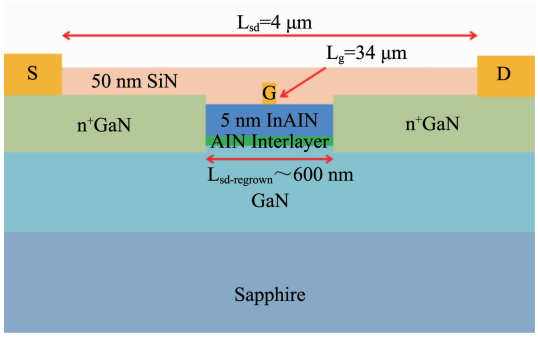



Fig. 1 Schematic cross section of the fabricated InAlN/GaN HFET
图1 InAlN/GaN HFET 器件横截面示意图

## 1 Experiments

Figure 1 shows the schematic cross section of the fabricated InAlN/GaN HFET. The InAlN/GaN heterostructure used in study was the same as the one in Ref. [12], which consists of a 5 nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier, a 1 nm AlN spacer, and a semi-insulating GaN buffer. The electron density and electron mobility of the as-grown material were measured to be $1.9 \times 10^{13}$ $cm^{-2}$ and 1 300 $cm^2/V \cdot s$, respectively, by employing van der Pauw structures at room temperature. The device processing was also same to Ref. [12], and further details on processing can refer to Ref. [12]. The drain-to-source distance between regrown regions (i.e., $L_{sd}$-regrown) was defined to be 600 nm, while the distance between source and drain electrodes was 4 μm. Based on our former experimental results, the source/drain-region dry etch and regrowth of Si-doped GaN were optimized to reduce the ohmic resistance. The Si doping

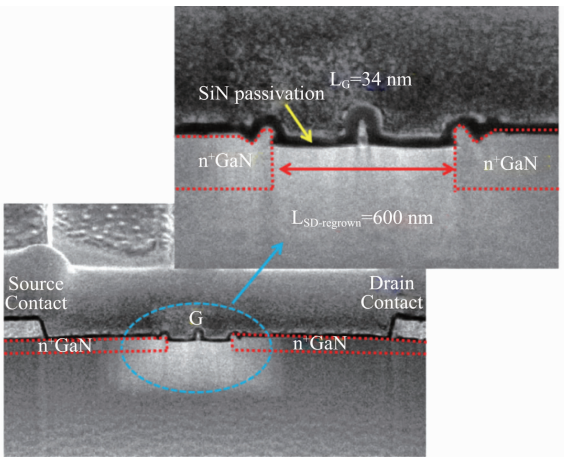



Fig. 2 Scanning Electron Microscope (SEM) cross-section image of the fabricated InAlN/GaN HFET
图2 InAlN/GaN HFET 器件横截面扫描电子显微镜(SEM)照片

concentration of the regrown $n^+$ GaN was increased to $7 \times 10^{19}$ $cm^{-3}$. A rectangular Ni/Au gate defined as 30 nm was in the center of the drain-to-source space by self-aligned e-beam lithography and lifted off technology. Finally, SiN passivation layer was deposited on the device surface by plasma enhanced chemic vapor deposition (PECVD).

The fabricated InAlN/GaN HFET was by cut perpendicularly to the gate by Focused Ion Beam (FIB), and the cross-section image gotten by Scanning Electron Microscope (SEM) was exhibited in Fig. 2. The drain-to-source distance between regrown regions (i.e., $L_s$d-regrown) and gate length were confirmed to be 600 nm and 34 nm, respectively, while the gate located in the center of the source-to-drain space.

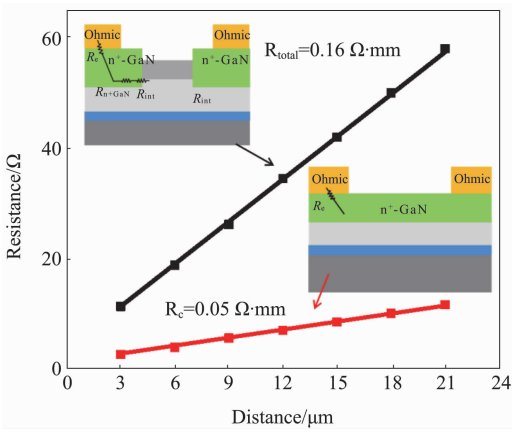



Fig. 3　Analysis of Ohmic resistances from TLM measurements

图 3　基于 TLM 测试的欧姆接触电阻分析

## 2　Results and discussions

As shown in the insertion of Fig. 3, the total resistance ($R_{tot}$) of the regrown $n^+$ GaN contact includes three parts: the interface resistance ($R_{int}$) between $n^+$-GaN and 2DEG, the $n^+$-GaN access resistance ($R_{n^+\text{-GaN}}$) between the regrown edge and ohmic metal, and the metal/$n^+$-GaN contact resistance ($R_c$). 100 μm × 100 μm quadrate patterns with different distance were fabricated on InAlN/GaN channel and regrown $n^+$-GaN channel, respectively. The transmission line method (TLM) measurements on the two different channels were taken and summarized in Fig. 3. In the analysis, all the dimensions of the patterns in TLM were confirmed by SEM. The total contact resistance ($R_{tot}$) of 0.16 Ω·mm and a sheet resistance of 251 Ω/sq were obtained from the TLM results on InAlN/GaN channel. The metal/$n^+$-GaN contact resistance ($R_c$) and $n^+$-GaN sheet resistance were extracted to be 0.05 Ω·mm and 50 Ω/sq, respectively, from the TLM results on $n^+$-GaN channel. Using the extracted $n^+$-GaN sheet resistance, the value of $R_{n^+\text{-GaN}}$ is counted to be about 0.02 Ω·mm. Finally, the interface resistance ($R_{int}$) between $n^+$-GaN and 2DEG is counted to be 0.09 Ω·mm. Table 1 summarizes the reported ohmic resistance of regrown $n^+$-GaN contacts. The total resistance ($R_{tot}$) of our sample is relatively low compared to other results, and gets a recorded low value among the ones regrown by MOCVD. It's also noteworthy that the value of $R_c$ (0.05 Ω·mm) is comparable with other reported values by MBE, and is the lowest in the reported values by MOCVD. The low value of $R_c$ is due to the high doping concentration of $n^+$ GaN, which is about $7 \times 10^{19}$ $cm^{-3}$. The value of $R_{int}$ (0.09 Ω·mm) is relatively high compared to other results, especially with the ones by MBE. The processes $n^+$ GaN material regrowth can be further improved, especially for the interface quality between $n^+$-GaN and 2DEG. Moreover, the crystalline damage cause by the etch process and the unintentional impurity induced by regrowth process would also be responsible for the interface resistance.

Based on the semiconductor characterization system, the output and transfer characteristics of the fabricated InAlN/GaN HFET were measured and shown in Fig. 4 (a) and (b), respectively. In the measurement of output characteristics, the gate voltage ranges from 1 V to -5V, stepped by -1V. As shown in the DC output curve, the fabricated device shows good pinch-off behavior. A maximum drain saturation current density ($I_{ds}$) reaches to 2.14 A/mm at $V_{gs}$ = 1 V, and the value of on-resistance ($R_{on}$) is extracted to be just 0.41 Ω·mm. Compared to our former results[12], the $R_{on}$ decreases obviously due to the improved ohmic contact. Moreover, the device shows obvious short-channel effects, as seen from an increased output conductance at $V_{ds}$ > 2 V and $V_{gs}$ <

**Table 1　Comparison of reported Ohmic resistances of regrown $n^+$ GaN contact by MBE and MOCVD**

**表 1　采用 MBE 和 MOCVD 方法外延 $n^+$ GaN 实现的欧姆接触电阻值对比表**

| Authors | Regrowth method | Material | $R_{total}$ (Ohm·mm) | $R_c$ (Ohm·mm) | $R_{int}$ (Ohm·mm) | |
|---|---|---|---|---|---|---|
| Yue Y Z, *et al* | MBE | InAlN/GaN | 0.16 | 0.06 | 0.08 | [10] |
| Guo J, *et al* | MBE | InAlN/GaN | 0.26 | 0.16 | 0.05 | [13] |
| Schuette M L, *et al* | MBE | InAlN/GaN | 0.1 | NA | NA | [14] |
| Shinohara K, *et al* | MBE | AlN/GaN | 0.085 | 0.026 | 0.026 | [5] |
| Brown D F, *et al* | MBE | AlGaN/GaN | 0.2 | NA | NA | [15] |
| Wu Y F, *et al* | MOCVD | AlGaN/GaN | 0.44 | NA | NA | [16] |
| Guo H Y, *et al* | MOCVD | AlGaN/GaN | 0.45 | 0.15 | 0.21 | [17] |
| Huang T D, *et al* | MOCVD | AlN/GaN | 0.27 | 0.153 | 0.056 | [18] |
| This work | MOCVD | InAlN/GaN | 0.16 | 0.05 | 0.09 | |

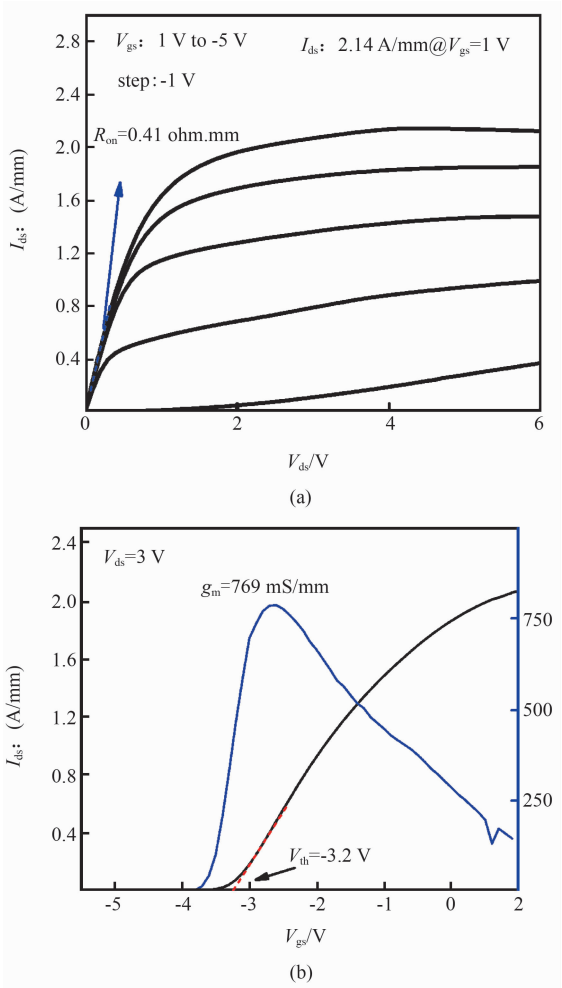
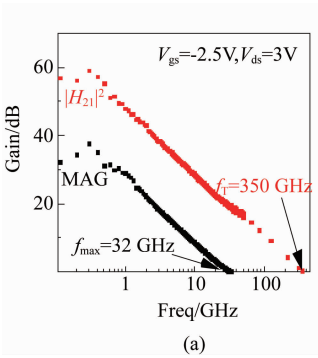



Fig. 4 DC output (a) and transfer (b) characteristics of the scaled InAlN/GaN HFET

图4 尺寸缩小的 InAlN/GaN HFET 器件直流输出(a)和转移(b)特性曲线




| | |
|---|---|
| $C_{gs}$ | 225 fF/mm |
| $C_{gd}$ | 150 fF/mm |
| $C_{ds}$ | 125 fF/mm |
| $g_{ds}$ | 150 fF/mm |
| $g_m$ | 807 fF/mm |
| $R_g$ | 80 Ω.mm |
| $R_s$ | 0.14Ω.mm |
| $R_d$ | 0.38Ω.mm |

Fig. 5 Small signal RF performance (a) and model parameters (b) of the prepared InAlN/GaN HFET

图5 InAlN/GaN HFET 器件射频小信号测试曲线(a)及器件模型参数(b)

−2 V. This is mainly due to reduction of the gate length. Moreover, increase of 2DEG electron density under the access region after SiN passivation may also enhance the SCEs. In the measurement of transfer curve, the drain bias is set as 3V, and the gate voltage ranges from 1V to −5.5 V, stepped by −0.1 V. The threshold voltage ($V_{th}$) obtained from the transfer characteristics is −3.2 V. A peak extrinsic transconductance ($g_m$) of 769 mS/mm is gotten.

The small-signal RF performance of the device was carried on wafer from 100 MHz to 50 GHz with 0.05 GHz step using a vector network analyzer. A Line Reflect Reflect Match (LRRM) calibration was used in the analyzer with off-wafer impedance standards. With on-wafer open/short calibration structures, parasitic pad inductances and capacitances were de-embed from the measured S-parameters[19]. Figure 5 (a) shows the de-embed current gain $|H_{21}|^2$ and the maximum available gain (MAG) plotted against frequency at the gate bias of −2.5 V and drain bias of 3 V. By −20 dB/dec roll off, the values of $f_T$ and $f_{max}$ are extrapolated to be 350 GHz and 32 GHz, respectively.

The expressions of current gain cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) are given as follows[3]:

$$f_T = \frac{1}{2\pi\left[\frac{L_g + \Delta L}{v_{sat}} + C_{gd}(R_s + R_d) + \tau_{cc}\right]} \approx \frac{v_{sat}}{2\pi L_g}, \quad (1)$$

$$f_{max} \approx \frac{f_T}{2\sqrt{(R_i + R_s + R_g)g_{ds} + (2\pi f_T)R_g C_{gd}}}, \quad (2)$$

where, $L_g$ represents the gate length, $\Delta L$ represents the effective expanding gate length, $v_{sat}$ represents the electron saturation velocity, $C_{gd}$ represents the gate-to-drain capacitance, $\tau_{cc}$ represents the channel charging time, $g_d$s is output conductance, $R_s$, $R_d$, and $R_g$ is the source, drain and gate resistance, while $R_i$ is the channel resistance. Compared to our former results ($f_T$ = 220 GHz@ 50 nm)[12], the value of $f_T$ increases effectively due to the decrease of gate length (34 nm). Moreover, as seen from the expression of $f_T$, the scaling of source-drain distance and improved ohmic contacts are also propitious to improve the RF characteristics. To our knowledge, the value $f_T$ of 350 GHz is the best reported for GaN-based HFETs in domestic. From the cold-FET and the measured S-parameters of the devices[17], the equivalent circuit model parameters were extracted and shown in Fig. 5 (b). Attributed to the effective scaling of source-to-drain distance and improved ohmic contacts, the values of channel resistance ($R_i$), source resistance ($R_s$) and drain resistance ($R_d$) are very small. However, as seen from the expression of $f_{max}$, the large value of $R_g$ induced by the rectangular Schottky gate, results in a poor value of $f_{max}$.

Figure 6 summarizes the reported $f_T$ vs $L_g$ in InAlN/GaN HFETs. The fabricated device shows a comparable high value of $f_T$ with 34 nm gate length. The electron saturation velocity ($v_{sat}$) in the GaN-based HFET can be calculated as: $v_{sat} = 2\pi L_g \times f_T$. The calculated values of electron saturation velocity in the reported InAlN/GaN HFETs are also plotted in Fig. 6. The value of $v_{sat}$ in the

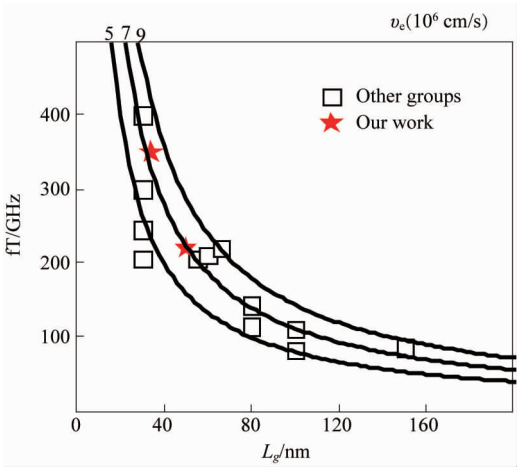



Fig. 6　Comparison of measured $f_T$ vs $L_g$ with other groups
图 6　与其他研究组报道的 $f_T$ 与 $L_g$ 关系对比图

fabricated device is the same as our former results.[12] This is mainly because of the same material and device processing. Moreover, the value of $\nu_{sat}$ of our device is in a comparable high level, which is just little lower than the highest one ($0.9\times10^7$ cm/s). However, the calculated $\nu_{sat}$ value is much lower than the theoretical one $3\times10^7$ cm/s.[18] This is mainly because that the calculated $\nu_{sat}$ value is extrinsic, which does not consider the influence of all the parasitical parameters. Moreover, the crystal quality also affects the electron saturation velocity.

## 3　Conclusions

In summary, scaled InAlN/GaN HFET with high $f_T$ were fabricated using nonalloyed Ohmic contacts. In the fabricated device, the drain-to-source distance ($L_{sd}$) was reduced to 600 nm, and rectangular gate length was reduced to 34 nm. Moreover, Ohmic resistance was improved by processing optimization of dry etching and $n^+$-GaN regrowth. The electrical characteristics of the devices were improved greatly after the reduction of ohmic resistance and gate length. A high drain saturation current density of 2.14 A/mm at $V_{gs}=1$ V was obtained, and the peak extrinsic transconductance ($g_m$) of 769 mS/mm was gotten. On-wafer small-signal measurements indicate that the device with 34-nm rectangular gate shows a high $f_T$ of 350 GHz.

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