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60 nm T-shaped-gate InAlN/GaN HFETs with f_T & f_{max} of 170 & 210 GHz

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Abstract: Scaled InAlN/GaN heterostructure field-effect transistors (HFETs) on sapphire substrate with high unity current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were fabricated and characterized. In the device, scaled source-to-drain distance (L_{sd}) of 600 nm was realized by employing nonalloyed regrown n^+-GaN Ohmic contacts. Moreover, a 60-nm T-shaped gate was fabricated by self-aligned-gate technology. A high drain saturation current density (I_{ds}) of 1.89 A/mm @ V_{gs} = 1 V and a peak extrinsic transconductance (g_m) of 462 mS/mm were obtained in the scaled InAlN/GaN HFETs. In addition, from the small-signal RF measurements, the values of f_T and f_{max} for the device with 60-nm gate were extrapolated to be 170 GHz and 210 GHz at the same bias. To our knowledge, they are the highest values of f_T and f_{max} for the domestic InAlN/GaN HFETs.

Key words: InAlN/GaN, heterostructure field-effect transistors (HFET), unity current gain cut-off frequency (f_T), maximum oscillation frequency(f_{max})

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基于 60 nm T 型栅 f_T & f_{max} 为 170 & 210 GHz 的 InAlN/GaN HFETs 器件

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摘要:基于蓝宝石衬底 InAlN/GaN 异质结材料研制具有高电流增益截止频率(f_T)和最大振荡频率(f_{max})的 InAlN/GaN 异质结场效应晶体管 (HFETs). 基于再生长 n^+ GaN 欧姆接触工艺实现了器件尺寸的缩小,有效源漏间距(L_{sd})缩小至 600 nm. 此外,采用自对准栅工艺制备 60 nm T 型栅. 由于器件尺寸的缩小,在 V_{gs} = 1 V 时,器件最大饱和电流(I_{ds})达到 1.89 A/mm,峰值跨导达到 462 mS/mm. 根据小信号测试结果,外推得到器件的 f_T 和 f_{max} 分别为 170 GHz 和 210 GHz,该频率特性为国内 InAlN/GaN HFETs 器件频率的最高值.

关 键 词:InAlN/GaN;异质结场效应晶体管(HFETs);电流增益截止频率(f_T);最大振荡频率(f_{max})

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Introduction

Lattice-matched InAlN/GaN heterostructure field-effect transistors (HFETs) have attracted great attention in the past several years because of their high two-dimensional electron gas (2DEG) density with an ultra-thin barrier, and potential reliability advantages[1-2]. Compared with AlGaN/GaN heterostructure, the strong spontaneous polarization in InAlN/GaN heterostructure not only leads to a high drain current, but also effectively suppresses the short channel effects (SCEs) due to the ultra-thin InAlN gate layer. The InAlN/GaN heterostructure has been proposed as an ideal alternative for device scaling to improve the RF characteristics. Moreover, since without piezoelectric polarization in the lattice-matched InAlN/GaN heterostructure, the defects can be reduced, offering a solution to strain-related device reliability.

In recent years, outstanding improvements in the

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frequency performance of InAlN/GaN HFETs have been achieved. Lee *et al* employed oxygen plasma treatments to reduce RF transconductance (g_m) collapse, and fabricated a 30 nm gate-length InAlN/GaN HFET with unity current gain cut-off frequency (f_T) of 245 GHz[3]. They then introduced InGaN back barrier to suppress the SCEs, and improved the value of f_T to be 300 GHz[4]. Using regrown Ohmic contacts, Yue *et al* reduced the source-to-drain distance (L_{sd}) to 270 nm, and reported a high f_T of 400 GHz in an ultrascaled InAlN/GaN HFET with a gate length of 30 nm[5]. However, the values of maximum oscillation frequency (f_{max}) in the above devices were very low due to the large gate resistance (R_g) induced by the rectangular gate, limiting its use in practical high-power amplifier applications.

Song *et al* employed a 30 nm T-shaped gate to reduce the gate resistance (R_g), and fabricated an InAlN/GaN HFET with f_T/f_{max} of 194/220 GHz[6]. Tirelli *et al*. obtained an InAlN/GaN HFET with f_T/f_{max} of 205/220 GHz using 30 nm Y-shaped gate[7]. Using regrown Ohmic contacts, the source-to-drain distance (L_{sd}) was scaled to 140 nm by Schuette *et al*, and the values of source resistance (R_s), drain resistance (R_d) and channel resistance (R_i) were reduced greatly. A recorded f_T/f_{max} of 302/301 GHz was obtained in a D-mode InAlN/GaN HFET with a gate length of 27 nm[8]. Our group fabricated a 70 nm T-shaped InAlN/GaN HFET with 162-GHz f_T and 176 GHz f_{max} using alloyed Ohmic contacts[9]. The great improvements in the frequency performance allow the InAlN/GaN HFETs in power-amplifier applications above W-band.

In this work, we report fully passivated InAlN/GaN HFETs with f_T/f_{max} of 170/210 GHz. This high RF performance is enabled by a gate lithography process to fabricate 60-nm T-shaped electrodes while maintaining a closing-300-nm-wide head in order to minimize gate resistance (R_g). In addition, regrown n^+-GaN Ohmic contacts were adopted to scale the source-to-drain distance (L_{sd}) to 600 nm, which reduced the parasitical resistances. The fabricated InAlN/GaN HFETs also show good DC characteristics. The maximum drain saturation current density (I_{ds}) reaches a value of 1.89 A/mm at $V_{gs}=1$ V and a peak extrinsic transconductance (g_m) of 462 mS/mm is obtained.

1 Experiments

As shown in Fig. 1, the InAlN/GaN heterostructure for this study was grown on (0001) sapphire substrate by metal-organic chemical vapor deposition (MOCVD). Epilayers consist of a 5 nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier layer, a 1 nm AlN spacer, and a semi-insulating GaN buffer. As measured using van der Pauw structures at room temperature, the as-grown material produced a 2DEG with a total charge density of 1.9×10^{13} cm^{-2} and an electron mobility of 1 300 $cm^2/V\cdot s$, resulting in a sheet resistance of 253 Ω/□.

Device processing started with mesa isolation, which was performed using a Cl_2/BCl_3 plasma-based dry etching. Subsequently, the InAlN/GaN heterostructure was deposited with SiO_2 mask for n^+-GaN ohmic regrowth by plasma enhanced chemic vapor deposition (PECVD) and patterned using reactive ion etching (RIE). A regrowth well-to-well distance (i.e., $L_{sd\text{-}regrown}$) of 600 nm was defined to reduce the parasitic resistance and capacitance. The n^+ GaN was regrown by MOCVD with a Si doping level of $\sim3\times10^{19}$ cm^{-3}. The n^+ GaN on top of SiO_2 was lifted off by HF after regrowth. Ti/Au metal stack was deposited as Ohmic contacts. Using the transmission line method (TLM) measurements, the total Ohmic resistance (R_{tot}) was measured to be 0.38 Ω·mm, including metal/n^+-GaN contact resistance (R_c), n^+-GaN access resistance between the regrown edge and ohmic metal ($R_{n+\text{-}GaN}$), and the resistance (R_{int}) at interface of n^+-GaN/2DEG. In the analysis, all the dimensions of the patterns in TLM were confirmed by SEM. The higher value of R_{tot} than other reported results is mainly because of a low Si doping level. Moreover, the sidewall obliquity near the regrown interface induced by the plasma dry etching also affects the value of R_{int}, which further increases the total Ohmic resistance[10]. Using a trilayer photoresist, electron-beam lithography was employed to define a 60nm T-shaped gate which is self-aligned to the n^+-GaN nonalloyed ohmic contacts. The Schottky gate is in the center of the source-to-drain space. Finally, SiN passivation layer was deposited by PECVD and patterned for contact pads using RIE. Figure 2 (a) shows the cross-sectional scanning electron micrograph (SEM) image of the T-shaped gate for the fabricated InAlN/GaN HFETs. The footprint is conformed to be 60 nm, while maintaining a 300-nm wide head in order to minimize gate resistance. Moreover, as shown in Fig. 2 (b), the distance between the regrown n^+ GaN contacts is conformed to be 600 nm, while the Schottky gate is in the center between the source and drain contacts.

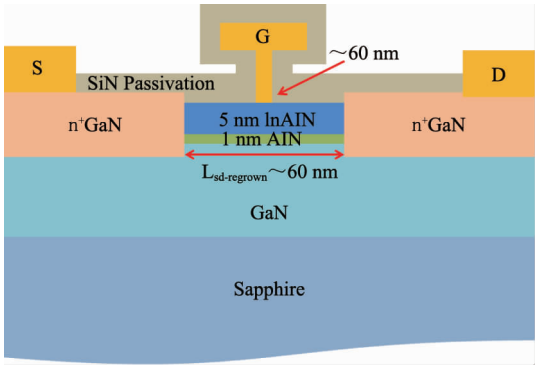

Fig. 1 Schematic cross section of the InAlN/GaN HFETs
图1 InAlN/GaN HFETs 器件截面示意图

2 Results and discussion

Using a semiconductor characterization system, the DC output characteristics of the fabricated InAlN/GaN HFET were measured and shown in Fig. 3. In the measurements, the drain-source voltage ranges from 0 V to 7 V, with a step of 0.05 V, while the gate bias ranges from 1 V to -6 V, with a step of -1 V. A maximum drain

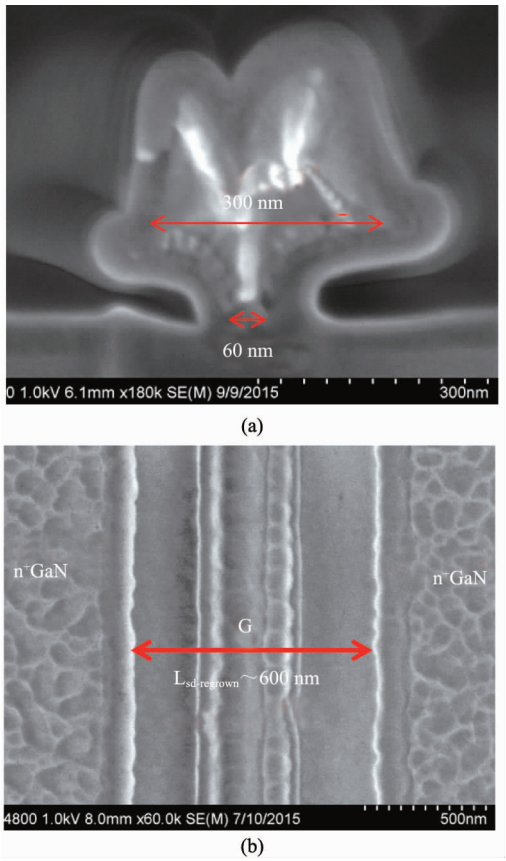

Fig. 2　Cross-sectional SEM image of the 60-nm T-shaped gate (a), and planform of the fabricated InAlN/GaN HFET (b)

图 2　(a) 60 nm T 型电镜截面图,(b) InAlN/GaN HFET 器件俯视图

saturation current density (I_{ds}) of 1.89 A/mm was obtained at V_{gs} = 1 V. The value of on-resistance (R_{on}) for the fabricated device was extracted to be 1.35 Ω · mm at V_{gs} = 1 V. This R_{on} value is higher than the total sum of the channel resistance and source/drain resistances (R_s + R_d + R_{sheet} = 1.21 Ω · mm) calculated based on the TLM results. The origin of the additional 0.14 Ω · mm may be due to the effect of gate metal or electric field on the channel electron density, which induces the increase of channel resistance. The high value of drain saturation current density and low value of R_{on} are mainly due to the effective scaling of source-to-drain distance. As seen from Fig. 3, the device shows good pinch-off behavior. However, although the ratio of gate length to InAlN barrier layer is larger than 9, some evidence of short-channel effects was observed as can be seen from an increased output conductance at V_{ds} > 4 V and V_{gs} < -2 V. This may be a result of the increase of 2DEG electron density under the access region after SiN passivation.

The transfer characteristics of the fabricated InAlN/GaN HFETs are shown in Fig. 4. In the measurements, the drain bias is set as 6 V, and the gate voltage ranges from 1 V to -6 V, with a step of -0.05 V. A peak extrinsic transconductance (g_m) of 462 mS/mm was obtained at V_{gs} = -2.75 V. The threshold voltage (V_{th}) extracted from the transfer characteristics is -4.1 V. Although the

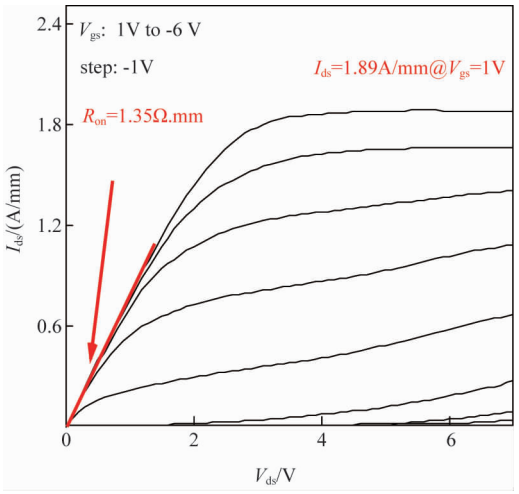

Fig. 3　Output characteristics of InAlN/GaN HFETs with regrown n^+-GaN contacts

图 3　采用再生长 n^+-GaN 欧姆接触的 InAlN/GaN HFETs 器件输出特性曲线

scaled device shows high drain saturation current density, the peak transconductance are relatively low at drain bias of 6 V. This is mainly because of the serious short-channel effects induced by the increase of 2DEG electron density under the access region after SiN passivation.

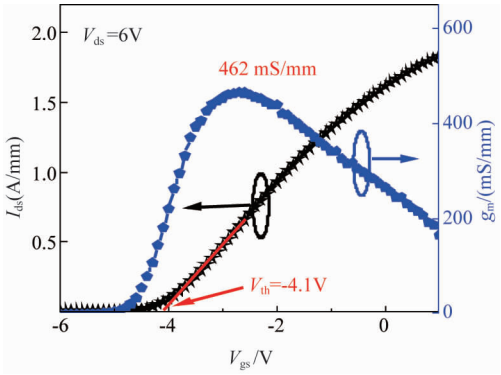

Fig. 4　Transfer characteristics of InAlN/GaN HFETs with regrown n^+-GaN contacts

图 4　采用再生长 n^+-GaN 欧姆接触的 InAlN/GaN HFETs 器件转移特性曲线

Figure 5 shows the three-terminal breakdown characteristics of the fabricated InAlN/GaN HFETs. During the measurement, the gate bias is set as -6 V while increasing the drain bias. As can be seen from Fig. 5, the off-state breakdown voltage (V_{br}) is 12.9 V, indicating the gate - drain breakdown voltage to be 18.9 V. These values correspond to the gate-drain breakdown field of ~0.73 MV/cm, which is much lower than the GaN critical field of ~3.4 MV/cm, also lower than the reported one (~3.3 MV/cm) in InAlN/GaN HFETs[8]. The leakage current of mesa isolation was 7×10^{-9} A/mm at bias of 15 V, while the leakage current increased to 7.8×10^{-9} A/mm after SiN passivation. This demonstrates that the SiN dielectric shows good insulation. The low breakdown characteristics may be mainly because of the traps at the

interface of SiN/InAlN, which adds leakage channel. In addition, the traps in the GaN buffer will also affect the breakdown characteristic due to the large lattice mismatch between GaN and sapphire substrate.

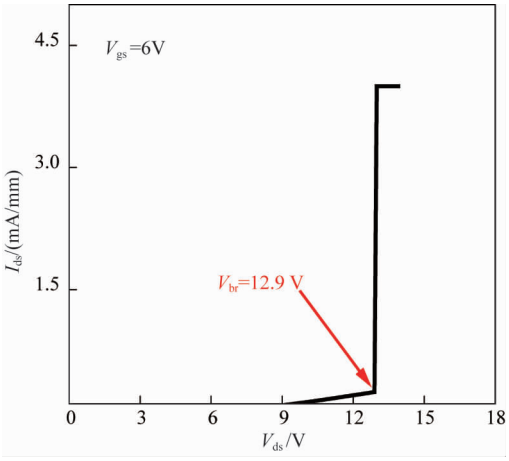

Fig. 5 The curve of three-terminal breakdown for the InAlN/GaN HFETs

图 5 InAlN/GaN HFETs 器件三端击穿特性曲线

The small-signal RF measurements of the InAlN/GaN HFETs were carried from 100 MHz to 50 GHz with a 0.05 GHz step using a vector network analyzer. The system was calibrated with an off-wafer line reflect match calibration standard. The measured S-parameters were de-embed using on-wafer open/short calibration structures.[11]. Figure 6 (a) characterizes the current gain $|H_{21}|^2$ and the maximum available gain (MAG) derived from measured S-parameters plotted against frequency at V_{gs} of -2.75 V and V_{ds} of 6 V. Extrapolation of $|H_{21}|^2$ and MAG -20 dB/dec roll-off yields f_T of 170 GHz and f_{max} of 210 GHz. To our knowledge, this is a recorded f_T/f_{max} of 170/210 GHz for InAlN/GaN HFETs in domestic. The high RF performance is mainly due to the scaling of source-to-drain distance, which effectively reduces the values of source resistance (R_s), drain resistance (R_d) and channel resistance (R_i). Moreover, the introduced 60-nm T-shaped gate not only increases the value of f_T, but also reduces the value of R_g, improving the maximum oscillation frequency.

Table 1 The main extracted equivalent circuit parameters, and comparison of measured and calculated f_T/f_{max}

表 1 提取的等效电路本征参数,以及 f_T/f_{max} 测试值和计算值的对比

Intrinsic Parameters	Measured f_T	Calculated f_T
$g_{m,i}$ = 590 mS/mm C_{gs} = 465 fF/mm C_{gd} = 68 fF/mm	170 GHz	176 GHz
g_{ds} = 84 mS/mm R_i = 1.15 Ω · mm R_g = 0.30 Ω · mm R_s = 0.42 Ω · mm	Measured f_{max} 210 GHz	Calculated f_{max} 208 GHz

The main intrinsic parameters of equivalent circuit

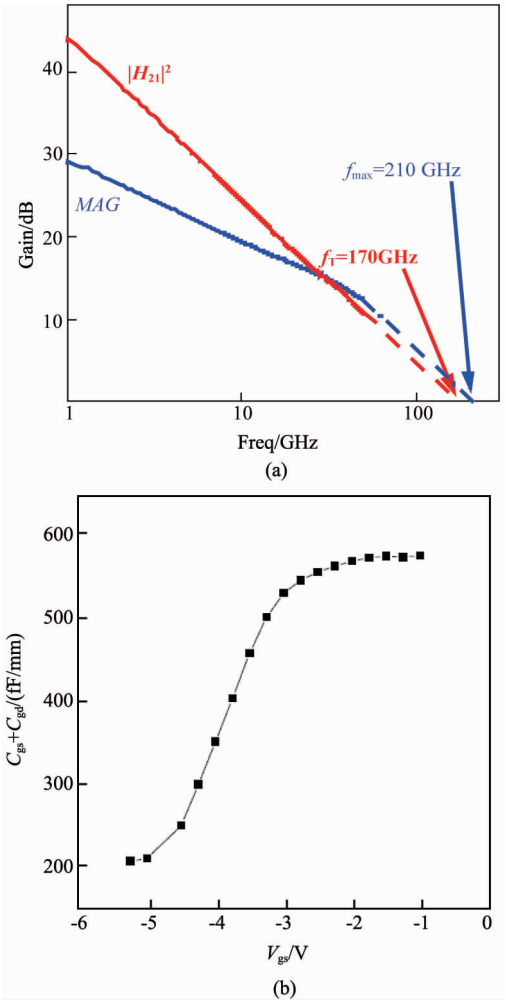

Fig. 6 Small signal RF performance (a) and the extracted capacitance-voltage characteristics (b) of the prepared InAlN/GaN HFETs

图 6 (a) InAlN/GaN HFETs 器件小信号射频特性,(b) 提取的电容电压特性曲线

obtained from the measured S-parameters are shown in Table 1. The expressions of f_T and f_{max} can be given as following[4]:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad , \quad (1)$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_i+R_g+R_s)g_{ds}+2\pi f_T R_g C_{gd}}} \quad , \quad (2)$$

where $g_{m,i}$ is the intrinsic transconductance, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, R_i, R_g, R_s, and g_{ds} represent the gate-charging, gate, source, and output resistance, respectively. The variations of the extracted values of $C_{gs}+C_{gd}$ with gate biases at V_{ds} of 6 V are shown in Fig. 6(b). The value of C_{gs} is comparable large due to the thin InAlN barrier layer. Moreover, the thick SiN passivation will also increase the value of C_{gs}. As shown in Table 1, the calculated values of f_T and f_{max} show good agreement with the measured ones, respectively. This demonstrates the accuracy of the equivalent circuit model of our device.

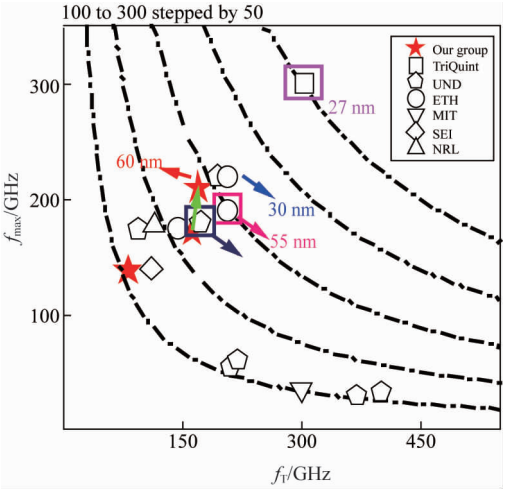

Fig. 7　f_T vs f_{max} for the reported InAlN/GaN HFETs
图 7　已报道的 InAlN/GaN HFETs 器件 f_T 和 f_{max} 汇总图

Some reported results of f_T vs f_{max} for the InAlN/GaN HFETs from different groups are summarized in Fig. 7[2-9, 12-15]. Many InAlN/GaN HFETs with f_T above 150 GHz, exhibit the values of f_{max} less than 60 GHz, resulting in a poor values of $\sqrt{f_T \cdot f_{max}}$ around 100 GHz. The rectangular-shaped gate used in these studies induces a high gate resistance limiting the value of f_{max}. The value of $\sqrt{f_T \cdot f_{max}}$ for our InAlN/GaN HFETs is nearly 200 GHz. The reported values of $\sqrt{f_T \cdot f_{max}}$ larger than 200 GHz are obtained with gate length of 30 nm or sun-30 nm. The value of $\sqrt{f_T \cdot f_{max}}$ is the highest one reported for InAlN/GaN HFETs with 60 nm gate length so far. Moreover, the f_T/f_{max} of 170/210 GHz is also very high for InAlN/GaN HFET on sapphire substrate. Figure 8 also shows the development for the InAlN/GaN HFETs of our group. Using alloyed Ohmic contacts, InAlN/GaN HFET with 100-nm T-shaped gate was fabricated, exhibiting f_T/f_{max} of 81/138 GHz. Gate length was then reduced to 70 nm, the values of f_T/f_{max} were improved to 162/176 GHz in an InAlN/GaN HFET with 2-μm source-to-drain space. Regrown n^+-GaN Ohmic contacts were employed to scale the source-to-drain distance (L_{sd}) to 600 nm, which effectively reduced the parasitical resistances. The InAlN/GaN HFET with 60-nm T-shaped gate exhibited f_T/f_{max} of 170/210 GHz. To further improve the RF characteristics, the gate length needs to be reduced. In addition, the Ohmic resistance of the regrown n + -GaN Ohmic contacts is much larger than the reported ones, and needs to optimize the regrowth of n^+ GaN to reduce the resistance.

3　Conclusions

In summary, we fabricated and characterized an InAlN/GaN HFET with high values of f_T and f_{max} on sapphire substrate. In order to reduce the parasitical resistance, including R_d, R_s and R_i, the source-to-drain distance (L_{sd}) was scaled down to 600 nm using n^+-GaN Ohmic contacts. In addition, a 60-nm T-shaped gate was fabricated by self-aligned-gate technology in the middle of the source and drain contacts. Due to the scaled source-to-drain distance, the InAlN/GaN HFET showed a high I_{ds} of 1.89 A/mm @ V_{gs} = 1 V and a peak g_m of 462 mS/mm. On-wafer small-signal RF measurements indicates that the values of extrapolated f_T and f_{max} for the device were 170 GHz and 210 GHz, respectively. To the best of our knowledge, the values of f_T and f_{max} are the best domestic reported for InAlN/GaN HFETs.

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