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150 GHz and 180 GHz fixed-tuned frequency multiplying sources with planar Schottky diodes

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Abstract: We report on the design and evaluation of two frequency bandwidth multiplying sources with planar Schottky diodes mounted on quartz thin film circuit. Novel co-simulation approach is used. Full-wave analysis is utilized to find diode deembedding impedances with lumped port to model the nonlinear junction. The doubler circuit is divided into several matching parts for ease of design. Individual parts of the doubler are independently designed and then these parts are combined and optimized simultaneously. The exported S-parameters of the whole circuit are used for multiplying efficiency analysis. For the 150 GHz doubler, the highest measured efficiency is 7.5% at 149.2 GHz and the typical efficiency is 6.0% in 147.4 ~ 152 GHz. As for the 180 GHz doubler, the highest measured efficiency is 14.8% at 170 GHz and the typical value in 150 ~ 200 GHz is 8.0%.

Key words: frequency doubler; planar Schottky diode; harmonic balance analysis (HBA); efficiency
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基于肖特基平面二极管的150 GHz和180 GHz固定调节式倍频源

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摘要:利用GaAs肖特基平面二极管,基于石英薄膜电路工艺,采用场和路相结合的综合分析方法,研制出了两个不同频率带宽的倍频器.在场软件中,二极管非线性结采用集总端口模拟,以提取二极管的嵌入阻抗,设计二倍频器的无源匹配电路,优化倍频的整体电路性能,提取相应的S参数文件,分析倍频器的效率.150 GHz二倍频器在149.2 GHz测得最高倍频效率7.5%,在147.4~152 GHz效率典型值为6.0%;180 GHz二倍频器在170 GHz测得最高倍频效率14.8%,在150~200 GHz效率典型值为8.0%.

关 键 词:二倍频器;肖特基平面二极管;谐波平衡分析;效率
中图分类号:TN773.2 **文献标识码**:A

Introduction

Terahertz covers frequency band between infrared and millimeter waves. This electromagnetic spectrum is attractive because terahertz wave sources can be used for a variety of applications such as molecular spectroscopy, atmospheric remote sensing, scaled radar range systems, sensing and monitoring of chemical and biological molecules, etc. The wide spread utilization of terahertz band is very slow. The primary reason is due to the lack of broad band, high power, high stability and compact sources.

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Existing millimeter and terahertz wave sources technology is presented in detail, such as oscillator sources, photonic mixing and frequency multiplication. The fundamental millimeter and terahertz wave oscillators can be classified as either tube-type or as solid state. Vacuum and gas-filled tube sources (BWO, TWT and Magnetron) have the problems of weight, size and reliability issues, which have restricted its use for many applications. Consequently, advances in tube technology appear to have leveled off and new sources incorporating tubes are relatively few in number. Solid state oscillators can be classified into two terminal and three terminal devices. The power of two terminal solid state oscillators, such as GUNN and IMPATT is generally on the order of hundreds of milliwatts in millimeter[1-3], and decreases dramatically at increased frequency. The output power of three terminal devices such as HBT, HEMT, and recently developed SiGe CMOS and BiCOMS technology is low compared with two terminal devices, but superior in phase noise. Most of research work reveals that improvement in maximum operating frequency and output power of these devices is very slow[4-9]. Another method is photonic mixing and detection to generate millimeter and terahertz signals. The application of this technology is limited by commercial photo-detectors failing to respond faster than 50GHz. Based on above discussion to generate high efficiency, high output power, broad band, low noise and compact terahertz sources, frequency multiplication is a very effective way[10-17].

In this paper, two hybrid integrated frequency doublers are realized with GaAs Schottky diodes. All passive networks, such as low pass filter, E-plane waveguide to microstrip transition, input and output matching networks, and diode passive part are analyzed by EM simulator. The exported S-parameters of the optimized complete circuit are used for HBA in ADS. For the 150 GHz doubler, the highest measured multiplying efficiency is 7.5% at 149.2 GHz, and the typical efficiency is 6.0% in 147.4 ~ 152 GHz. For the 180 GHz doubler, the highest measured efficiency is 14.8% at 170 GHz, and the typical efficiency is 8.0% in 150 ~ 200 GHz.

1 Circuit Design

An iterative "divide and combine" co-simulation design approach was adopted. First the doubler circuit is divided into different parts, and then each part is simulated and optimized individually. Finally, the different parts are combined and optimized together. The co-simulation design process of the doubler is presented in Fig. 1.

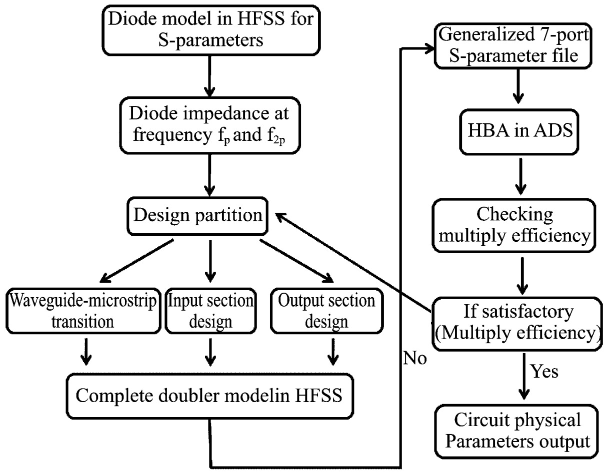

Fig. 1 Doubler design flow chart
图 1 二极管倍频器设计流程

1.1 Diode model deembedding impedances

A flip-chip planar Schottky varactor chip with four diodes integrated in antiseries configuration is adopted. The dimension of the diode is 0.26 mm × 0.05 mm × 0.018 mm (length, width and thickness, respectively), which can be comparable with operation wavelength, when operation frequency is high. The accurate modeling of the diode is a fundamental task for the doubler design. The diode is mounted as shown in Fig. 2, input signals is coupled to the diode with phase difference of 180°, the generated even harmonic signals are in-phase at the output port, and odd harmonic signals are out-of-phase and can't propagate to the output port. Therefore, the multiplying circuit can be balanced even for harmonic multiplication, as described in Fig. 3[10-11]. The ideal non-linear Schottky diode junction is modeled by SPICE parameters (C_{jo} = 0.01pF, $I_s = 1.5 \times 10^{-13}$ A, $R_s = 5\Omega$, $n = 1.15$). To accurately predict the diode optimum deembedding impedances, adding the influence of parasitics, a full-wave 3D EM simulation of the diode was carried out to find the optimum deembedding impedances. The material parameters used during modeling are depicted in table 1. The internal coaxial or lumped port probe method was used to represent the diode nonlinear junction and extract the S-parameters directly from electromagnetic simulation. The diode pad interface has been extruded and the transmission line ports are later deembedded back to the diode reference planes, as described in Fig. 2. The S-parameter file of the diode is exported for diode deembedding impedances discussion in ADS. By running HBA in ADS, the diode optimum impedances of input pump frequency and output second harmonic frequency are obtained ($Z_{fp} = 17 + j \times 46$, $Z_{f2p} = 26 + j \times 35$). The value of impedances will be used to synthesize the doublers.

Table 1 Diode material parameter values
表1 二极管材料参数

N^{++} GaAs epitaxial	Perfect conductor
N GaAs buffer layer ($\varepsilon_r = 12.9$)	Lossless dielectrics
GaAs substrate ($\varepsilon_r = 12.9$)	
SiO_2 layer ($\varepsilon_r = 4$)	

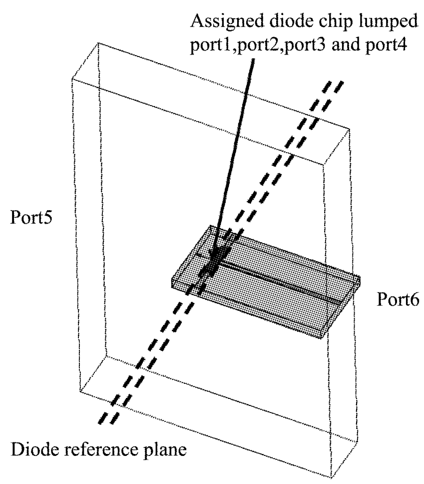

Fig. 2 Diode model in HFSS
图2 二极管 HFSS 模型

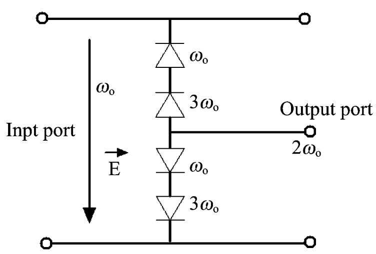

Fig. 3 Doubler schematic
图3 二倍频器原理图

1.2 Multiplying circuit optimization

The substrate for the multiplying circuit is quartz with dielectric constant of 3.78, and thickness of 0.08 mm. The circuit is presented in Fig. 4, the pump frequency TE_{10} is the only wave mode allowed to propagate in input circuit, while the effective input back short (L2) is turned for maximum transmission of pump signals to diode, with following reduced-width waveguide channel to sufficiently cut off the input TE_{10} mode. The length of the reduced-height waveguide (L1) and the location of the input back-short are optimized to achieve low return loss. The output section consists of the waveguide-microstrip transition, and the suspended strip quartz circuit, which can be divided into two parts. The first part next to the varactor chip (L2) is characterized by quasi-coaxial part, while the second part which forms the output deembedding circuit is a suspended strip line. The excited second harmonic is radiated in the unbalanced wave mode TEM, passes through the quasi-coaxial region between the varactor chip terminal and the input back-short, and then coupled into the output waveguide port with a succession of high and low impedance matching transmission lines. Therefore, the input and output circuit can be designed separately. A hammer type low pass filter connected with SMA for DC bias feeding, is used to prevent the leakage of second harmonic signals and present an open circuit to them.

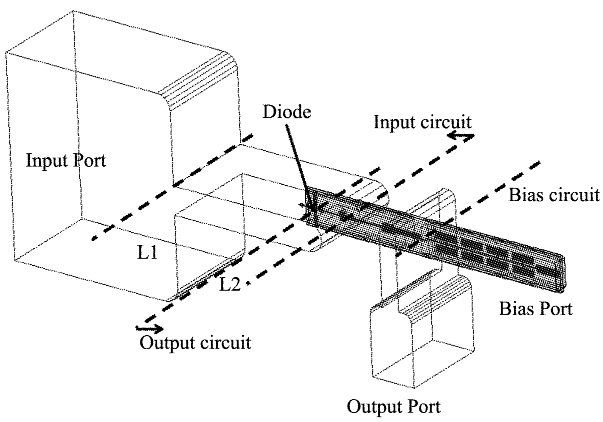

Fig. 4 Structure of the doubler circuit
图4 二倍频器电路结构

After all subcircuits had been optimized, the whole doubler circuit was analyzed. Seven port S-parameter file is extracted and then combined with nonlinear diode to model the multiplying efficiency, as shown in Fig. 5. This co-simulation process was repeated for further optimization. The optimized and fabricated quartz circuit is given in Fig. 6. The circuit was sawed by resin-bond dicing blades, and the blade is an excellent choice for hard and brittle materials sawing, especially for quartz glass.

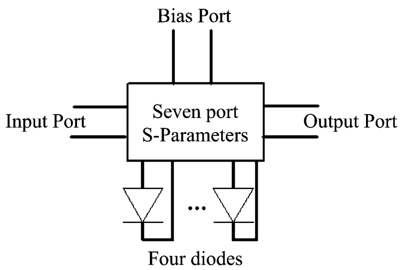

Fig. 5 Global optimization of the doubler
图 5 二倍频器整体优化仿真

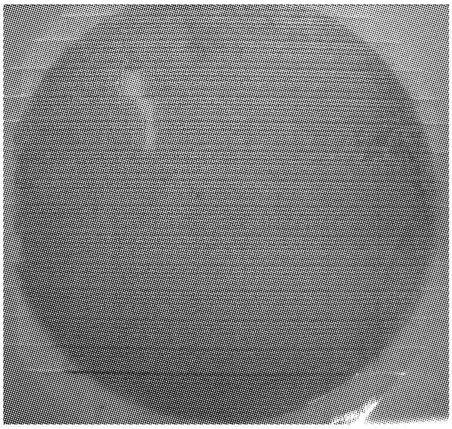

Fig. 6 Quartz circuit with 3 inch size
图 6 3 英寸石英电路

2 Experimental results

The quartz substrate was mounted to the waveguide block with silver epoxy. The split block was manufactured by brass and electroplate with gold. The split block photo is given in Fig. 7. The input and output port of 150GHz doubler are standard full-height WR-12 and WR-06 waveguides with waveguide dimensions of 3. 1 mm × 1. 55 mm and 1. 65 mm × 0. 83 mm, respectively. The input and output port of 180 GHz doubler are standard full-height WR-10 and WR-05 waveguides with waveguide dimensions of 2. 54 mm × 1. 27 mm and 1. 3 mm × 0. 65 mm, respectively. A SMA connector type KFD45 was connected to the end of bias port for DC feeding.

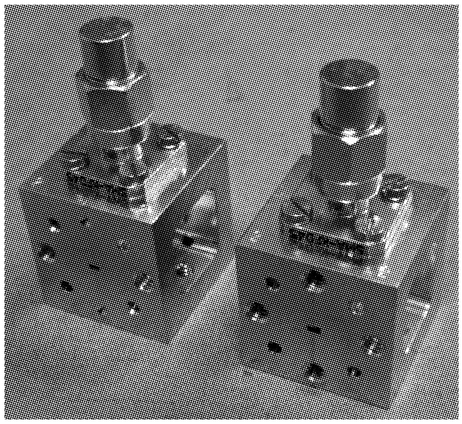

Fig. 7 Photo of the 150GHz and 180GHz doubler
图 7 150 GHz 和 180 GHz 二倍频器照片

The doubler measurement setup is presented in Fig. 8. The input power of doublers is provided by ELVA-1 BWO-W signal generator, and it is precisely calibrated by power meter PM-4. As described in Fig. 9, the highest measured multiplying efficiency of 150 GHz doubler is 7. 5% and corresponding output power is 2. 4mW at 149. 2 GHz with 32mW input power. Typical efficiency is 6% in 147. 4 ~ 152 GHz. In Fig. 11, the 180GHz doubler reaches a peak efficiency of 14. 8% at 170 GHz and output power is 7. 5mW at 170 GHz with input power of 50. 7mW. The typical efficiency is 8. 0% in 150 ~ 200 GHz. Good agreement was obtained between simulated and measured results. Fig. 10 and Fig. 12 show the measured output power as the function of input power. It can be seen, the multipliers reach peak efficiency at one fixed input power point. With the increasing of pump power, the output power of multipliers saturates and efficiency declines.

Table 2 illustrates commercial doubler products performance employing GaAs Schottky varactor diodes. Obviously, the multiplying efficiency of our designed doubler is 1. 5% lower than that of VDI products (VDI represents state-of-the art performance in Terahertz multiplying and mixing in word wide), but highest efficiency is superior and efficiency response as a function of frequency is broad band. The multipliers are attractive with hybrid integrated technology while comparing

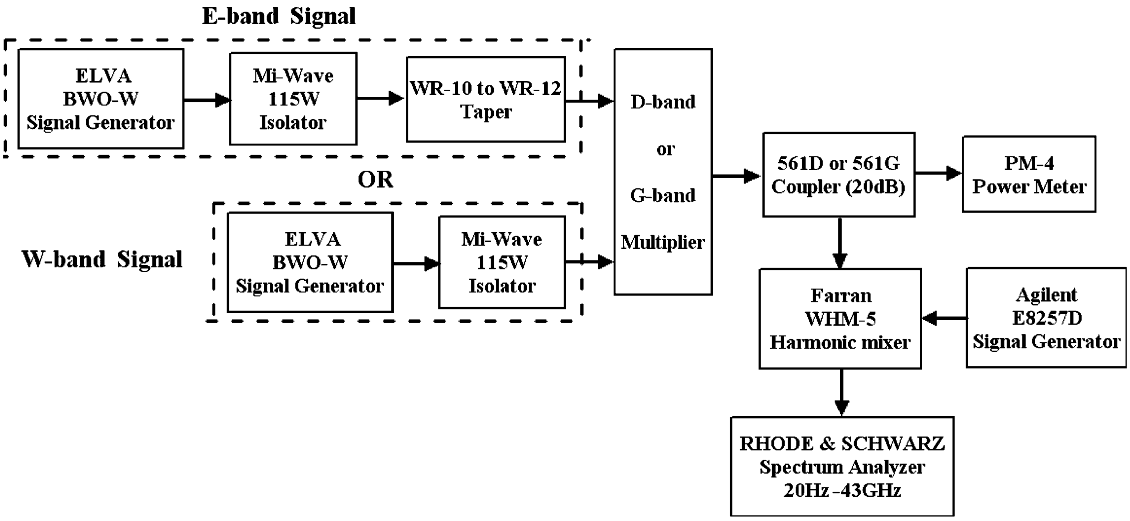

Fig. 8 Measurement setup of the doubler
图 8 二倍频器测试框图

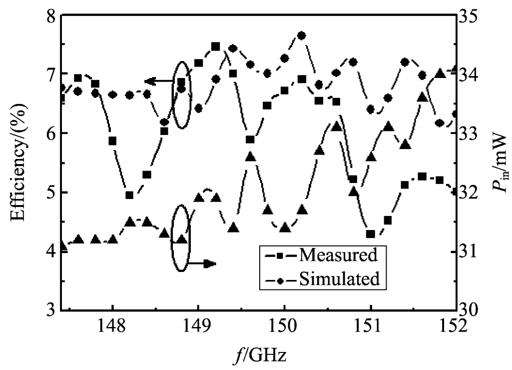

Fig. 9 Measured and simulated efficiency of the 150 GHz doubler
图 9 150 GHz 二倍频器仿真和测试效率

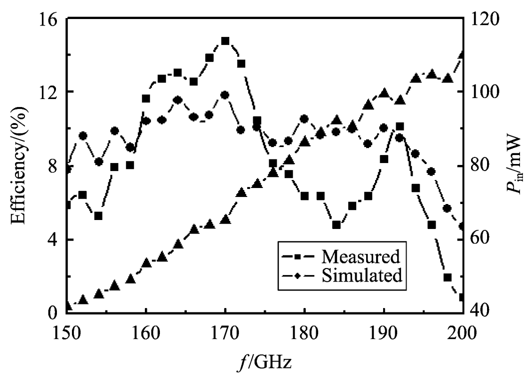

Fig. 11 Measured and simulated efficiency of the 180GHz doubler
图 11 180 GHz 二倍频器仿真和测试效率

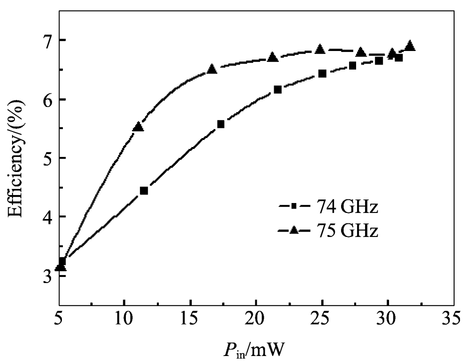

Fig. 10 Efficiency versus input power of the 150 GHz doubler
图 10 150 GHz 二倍频器效率和输入功率关系曲线

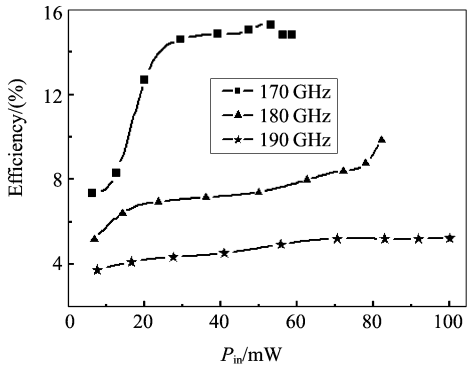

Fig. 12 Efficiency versus input power of 180 GHz the doubler
图 12 180 GHz 二倍频器效率和输入功率关系曲线

with commonly applied MMIC like quartz transferred technology. MMIC foundry based Schottky diodes transferred onto quartz substrate is complex and expensive[13], but it has low parasitic in terahertz. This work plays a solid foundation for future 220 GHz and 330 GHz frequency multiplying and mixing work.

Table 2 Performance comparison of the frequency doubler
表 2 二倍频器性能比较

Company	Model (D-band)	Efficiency	Model (G-band)	Efficiency
This paper	–	Typ 6%	–	Typ 8%, Max 14.8%
VDI	WR6.5×2	Typ7.5%	WR5.1×2	Typ 9.5%, Max 13%

3 Conclusions

Two frequency doublers with different bandwidth were analyzed and designed with planar barrier Schottky diode. Full-wave analysis was carried out to find diode deembedding impedances with lumped port to model the nonlinear junction. An iterative "divide and combine" design approach was adopted, breaking up the circuit into different parts, where each part is simulated and optimized individually. The different parts are then combined and optimized together. The exported S-parameters of the optimized circuit are used for multiplying efficiency analysis. To 150 GHz doubler, the highest measured efficiency is 7.5% at 149.2 GHz, and typical efficiency is 6.0% in 147.4 ~ 152 GHz. To 180 GHz doubler, the highest measured efficiency is 14.8% at 170 GHz, and typical efficiency is 8.0% in 150 ~ 200 GHz.

The doublers are simple, compact, low cost, fixed-turned, and high efficiency, which is very attractive for test instrument, frequency sources and corresponding application systems.

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