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0.5 μm InP/InGaAs DHBT for ultra high speed digital integrated circuit

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Abstract: 0.5μm InP/InGaAs DHBT with 350/533 GHz f_t/f_{max} and two layers of interconnecting technology were developed for ultra high speed digital integrated circuit (IC) application. A static divide-by-2 frequency divider operating at 100 GHz was demonstrated. As the important parameters of gate delay, base-collector capacitance C_{cb} and C_{cb}/I_C were analyzed. The value of C_{cb}/I_C as low as 0.4 ps/V was achieved, indicating that frequency divider operating above 150 GHz could be potentially realized.

Key words: InP, heterojunction bipolar transistor, static frequency divider
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用于超高速数字集成电路的0.5um InP/InGaAs双异质结晶体管

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摘要:报道了用于超高速数字集成电路的0.5 μm发射级线宽的InP/InGaAs DBHT器件,及其100 GHz的静态分频器,其工作频率达到国内领先.并详细分析了器件CB结电容对影响高速数字应用的影响,其中Ccb/Ic达到0.4 ps/V,揭示其静态分频器具有工作在150 GHz以上的潜力.

关 键 词:磷化铟;双异质结晶体管;静态分频器

中图分类号:TN3 **文献标识码**:A

Introduction

Advances in large capacity communication system and digital radar have stimulated intense research for devices operating at frequency over 100 GHz. Owning to high electron drift velocity compared with devices based on Si, GaAs or SiGe, InP/InGaAs DHBT is a suitable candidates for ultra high speed digital application [1]. In recent years, aggressive scaling has been achieved on InP based DHBT. The maximum oscillation frequency (f_{max}) has reached 1 THz [2]. However upper limit of operation frequency for a digital integrated circuit (IC) is not directly determined by f_t/f_{max}, but often relative to base-collector capacity C_{cb}. This is because that $C_{cb} \triangle V_{logic}/I_C$ is usually considered as the main delay term for a static frequency divider, which is often used as a benchmark circuit working at highest data rate in a given digital IC. Therefore, InP/InGaAs DHBT with smaller C_{cb}/I_C could support higher operating frequency for digital circuits.

Due to highly scaled InP HBT technology, frequency divider speed has been improved aggressively. M. D'Amore *et al.* has reported 200 GHz + static frequency divider based on 0.25 μm InP DHBT technology[3]. Divide-by-8 frequency divider operating at 204.8 GHz based on 0.25 μm InP HBT was also published by Z. Griffith *et al.* [4]. While frequency divider becomes faster by scaled HBT, discussions about relations between HBT device and its circuit performance are still handful. Meanwhile, highly scaled HBT devices required excessive fabrication steps such as e-beam lithography. 0.5 μm emitter InP DHBT can also achieved over 500 GHz f_{max} with relative simple processes[5].

In this paper, we present an InP/InGaAs DHBT with 0.5 μm emitter width and two interconnect layers technology dedicated for digital IC above 100 GHz. As a benchmark circuit, a static divide-by-2 frequency divider

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working at 100 GHz was demonstrated, which is to our knowledge the highest operating frequency ever reported in China. The prior highest operating frequency of frequency divider in China is 83 GHz, reported in 2014 by Y. T. Zhang [6]. Relations between high speed digital IC and device characteristics were discussed. C_{cb}/I_C as low as 0.4 ps/V was achieved, indicating potentially operating frequency above 150 GHz.

1 Design and Fabrication

The epitaxial structure was listed in Table 1. The composite collector consists of set-back layer, δ- doping layer, and InP collector layer. 50 nm InGaAs setback layer and 50 nm δ- doping layer were designed to eliminate the conduction band spike at B-C interface and to minimize the collector current blocking effect[7]. InP collector thickness was optimized to 150 nm for balance between B-C capacity C_{cb} and Kirk current density J_{kirk}. 35 nm thin base was designed to reduce transit time in base. Emitter width was scaled to 0.5 μm for a smaller base pedestal area, and thus a smaller C_{cb}. After three mesa processes, thin film resistances were deposited on InP substrate. Capacitances were also made on substrate using SiN_x as dielectric. Two levels of circuit interconnect were realized through Benzocyclobutene (BCB) planarization processes and metal deposition as depicted in Fig. 1.

Table 1 Layer structure of the InGaAs/InP DHBT
表 1 InGaAs/InP DHBT 材料结构

Layers	Material	Thichness/nm	Dopant
Emitter Contact	InGaAs	200	Si
Emitter	InP	200	Si
Base	InGaAs	35	C
Set-back	InGaAs	50	Si
δ-doping	InP	50	Si
Collector	InP	150	Si
Collector Contact	InGaAs	50	Si
Sub-collector	InP	200	Si
Etch-stop	InGaAs	10	ud
Substrate	InP		S. I.

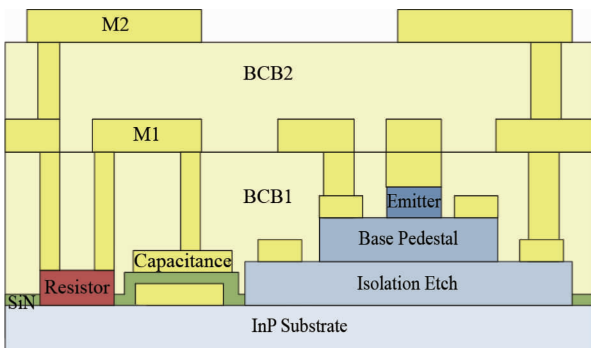
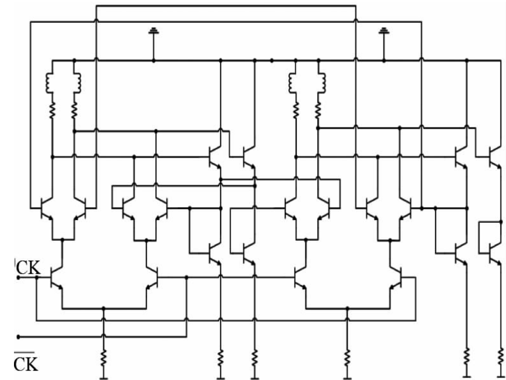
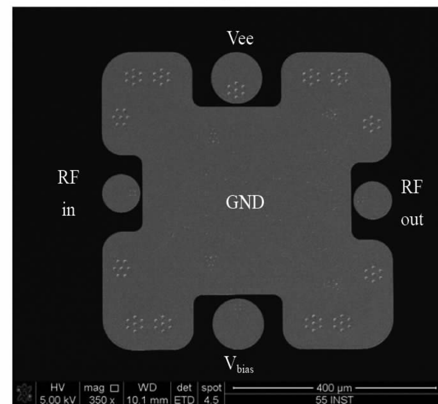


Fig. 1 Cross-section of the 0.5 μm InP/InGaAs DHBT for high speed digital IC
图 1 用于高速数字集成电路的 0.5 μm InP/InGaAs DHBT 剖面图

The divide-by-2 static frequency divider consists of input buffer, divider core and output stage. The Master-slave D-flip-flop works as the divider core, which employs emitter coupled logic (ECL), depicted in Fig. 2(a). 50 Ω on chip termination and peaking inductance were designed to decrease the interconnect delays. The circuit employs 32 DHBTs with an emitter area of 0.5 ×5 μm^2. The total area of the divider is about 500 × 500 μm^2. SEM of the static frequency divider is shown in Fig. 2(b).



(a)



(b)

Fig. 2 Frequency divider design: (a) divider core circuit; (b) SEM of the static frequency divider
图 2 分频器设计:(a)分频器核心电路;(b)静态分频器扫描电镜照片

2 Measurement

DC characteristics of single device were measured using Agilent 1500A semiconductor parameter analyzer. As depicted in Fig. 3(a), common emitter DC current gain of 33 was recorded at I_B = 450 μA. Extracted ideality factors for BE and BC junction are 1.67 and 1.07, respectively. *S*-parameters of the InGaAs/InP DHBT were characterized from 200 MHz to 67 GHz using PNA-X N5247A network analyzer. f_t and f_{max} were derived at different bias conditions. As shown in Fig. 3(b), f_t and f_{max} increase with emitter current I_E until reache the peak and then decrease, which was a consequence of *Kirk* effect. The highest f_t/f_{max} reaches 350/533 GHz at I_E = 9.4 mA, V_C = 1.5 V.

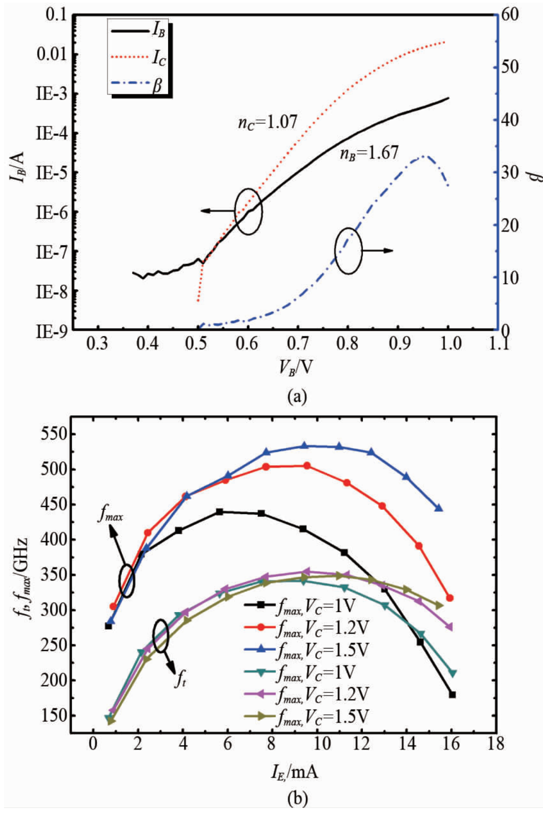


Fig. 3　Characteristics of the InGaAs/InP DHBT: (a) *MSG/MAG* and *U* of the DHBT; (b) variation of f_t and f_{max} versus I_C for the DHBT

图 3　InGaAs/InP DHBT 器件特性测量:(a) *MSG/MAG* 及 *U* 曲线;(b) f_t 和 f_{max} 随 I_C 的变化曲线

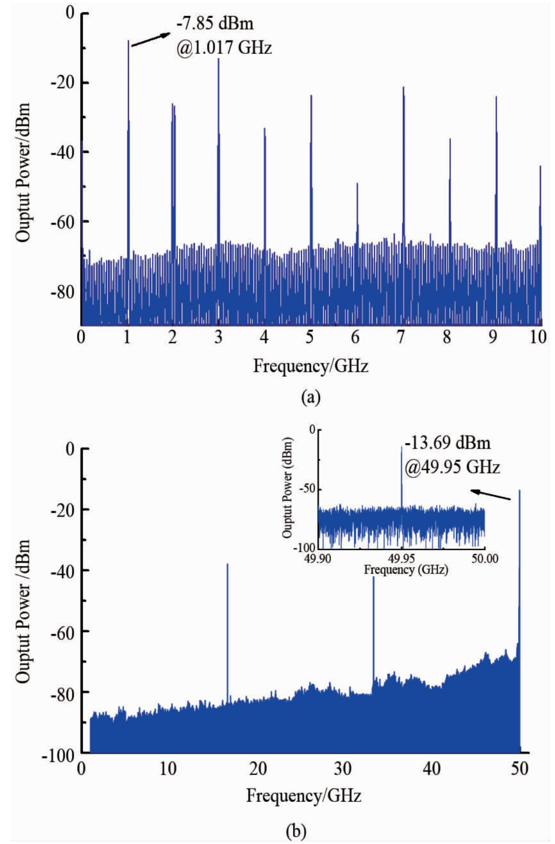


Fig. 4　Spectra of frequency divider output: (a) @ f_{clk} = 2 GHz; (b) @ f_{clk} = 100 GHz

图 4　分频器输出频谱:(a) f_{clk} = 2 GHz 时频谱;(b) f_{clk} = 100 GHz 时频谱

Limited by the measurement range of our 50 GHz spectrum analyzer, the frequency divider was characterized at clock frequency ranging from 2 GHz to 100 GHz. For 2 ~ 50 GHz, the signal source was used as the clock input directly. For 50 ~ 100 GHz, a frequency multiplier was applied. As shown in Fig. 4, the divider demonstrated 1 GHz output frequency at 2 GHz clock input and 50 GHz at 100 GHz input. Figure 5 shows that the characterized phase noise was-137.529 dBc/Hz at 100 kHz offset.

3　Discussion

The propagation delay of the divide-by-2 frequency divider can be deduced with the open circuit time constants method. $C_{cb}\triangle V_{logic}/Ic$ is the major delay part[8]. While $\triangle V_{logic}$ is 0.3 V for InP/InGaAs DHBT emitter coupled logic (ECL), decreasing C_{cb}/Ic directly promotes operating frequency. We firstly analyzed the C_{cb} and then discuss C_{cb}/Ic as follows.

Base-collector frequency C_{cb} can be affected by CB junction voltage V_{cb} and collector current density J_C, and written as [9]:

$$C_{cb} = \left| qN_C \cdot \frac{dx_n}{dV_{cb}} \right| - \left| \frac{J_C}{v} \cdot \frac{dx_n}{dV_{cb}} \right| - \frac{J_C}{v^2} \cdot \frac{dv}{dV_{cb}} \quad , \quad (1)$$

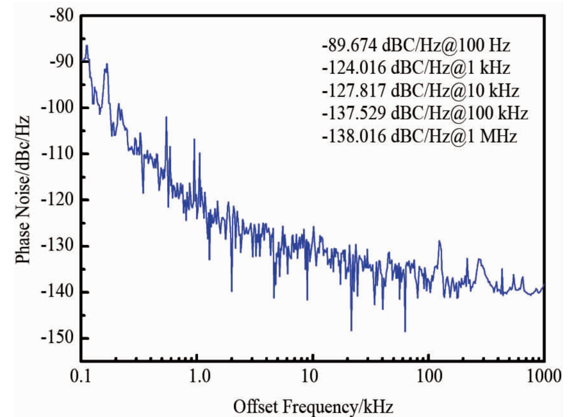


Fig. 5　Phase noise of the frequency divider

图 5　分频器相位噪声

where N_C is collector doping concentration, x_n is the thickness of depletion region. J_C is the collector current density, v is carrier velocity in collector. Thus the first term represents the variation of depletion region thickness. The following terms represent mobile charge modulation effect which represent injected electron density compensating doping concentration. C_{cb} can be derived

using Eq. 2 [10],

$$\mathrm{Im}\{Y_{12}\} = 2\pi f \cdot C_{cb} \quad , \quad (2)$$

where Y_{12} is transformed from S-parameters at a relative low frequency $f = 5$ GHz. The relationship of C_{cb}, collector voltage V_C and I_C is depicted in Fig. 6. As we can see, with the increase of voltage, C_{cb} drops due to increase of depletion region thickness. The mobile charge modulation effect leads to a decrease of C_{cb} with increase of I_C at relative small value region. However with J_C continuing to increase, C_{cb} begin to increase. The turning points reflect the screening of electric field at base side of the junction by the injected electrons. This is called *Kirk* effect.

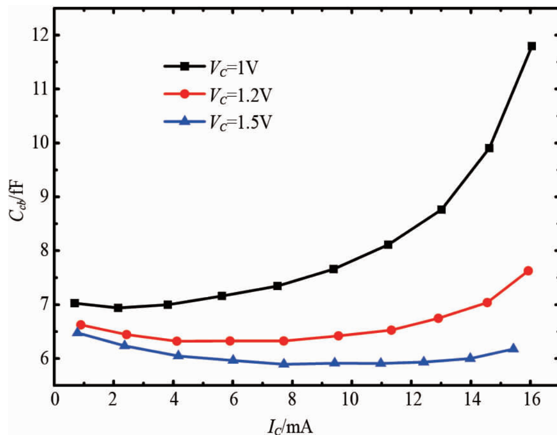


Fig. 6 Extracted C_{cb} versus I_C at different collector voltage V_C

图 6 不同集电极电压 V_C 下的 C_{cb} 比 I_C

C_{cb}/I_C versus I_C, as shown in Fig. 7, is similar with C_{cb} versus I_C except that the turning points locate in a much higher I_C. The smallest C_{cb}/I_C of 0.4 ps/V was recorded at $I_C = 15.4$ mA, $V_C = 1.5$ V. This value is even smaller than 0.59 ps/V reported in Ref. [11] by Z. Criffith *et al.* (UCSB), where a 150 GHz InP HBT static frequency divider was presented. Therefore, C_{cb}/I_C can be decreased by two approaches, decreasing C_{cb} by scaling device dimension and refining collector layer design or setting bias voltage at possible high level with proper current. In this paper, a small emitter area of 0.5 ×5 μm, compared with 0.7 ×10 μm in Ref. [6], and proper design of composite collector improved the frequency divider operating frequency from 83 GHz to 100 GHz. The recorded 0.4 ps/V of C_{cb}/I_C shows a potential operating frequency above 150 GHz at proper voltage and current bias. However limited by the measurement range of our spectrum analyzer, the highest operating frequency could not be recorded.

4 Conclusion

In summary, a 0.5 μm InP/InGaAs DHBT three mesa DHBT technology was developed for high speed frequency integration circuit application. DC current gain of 33 and f_t/f_{max} of 350/533 GHz was recorded. As benchmark of high frequency digital circuit, a divided-by-2 static frequency divider operating at 100 GHz was demonstrated. As the main delay term of the circuit, $C_{cb} \triangle V_{logic}/Ic$ was discussed. While $\triangle V_{logic}$ is about 0.3 V for ECL, C_{cb}/Ic represents the potential of the devices for high speed digital circuits. The smallest C_{cb}/Ic of 0.4 ps/V was recorded with our 0.5 μm InP/InGaAs DHBT, indicating a potential operating frequency above 150 GHz.

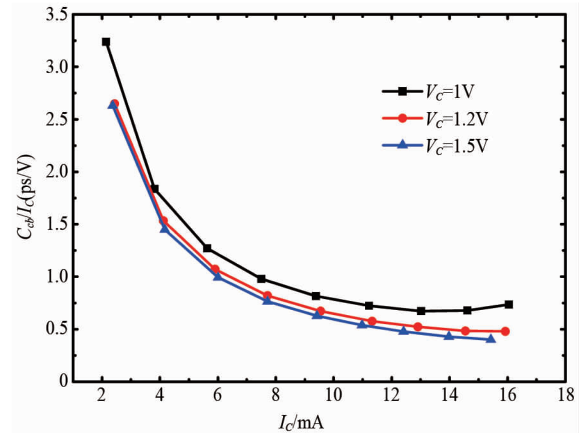


Fig. 7 C_{cb}/I_c vs. I_C at different collector voltage V_C

图 7 不同集电极电压 V_C 下的 C_{cb}/I_c 比 I_C

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